Dependence of Silicon Heterojunction Solar Cell Performance on Surface Preparation, Deposition Conditions, Chemical Treatment and Annealing

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Abstract- The effect of process parameters such as saw damage removal, gas dilution and silane depletion are studied to maximize the efficiency of silicon a-Si/c-Si heterojuction solar cells. Furthermore, the effect of chemical treatment and annealing are also studied to understand their effect on performance of silicon heterojunction solar cells. A smooth and defect free junction is required to exploit the heterojunction properties of the junction and produce high open circuit voltage. Hence a smooth c-Si surface and the incorporation and migration of hydrogen in the amorphous silicon layers, especially the intrinsic amorphous layer, are very important. The process parameters affecting these properties have been studied and direct relation between the process parameters and the cell performance has been found.

Keywords- Silicon Heterojunction, solar cells, Saw Damage Removal, Annealing, Silane

1. Introduction

Silicon heterojunction (HJ) solar cells have shown high efficiency in not only research laboratories but commercially as well [1]. The fabrication of HJ cells with n-type mono-crystalline silicon wafers requires the deposition of amorphous silicon layer on both sides of the wafer. The characteristic high voltage property of the HJ solar cells is mainly dependent upon the junction property at c-Si and intrinsic a-Si interface. The effects of various process parameters such as annealing and process gas flow have been observed on the overall efficiency of the solar cell. The availability and migration of hydrogen have been cited as the key factor for improving the cell efficiency [2, 3].

2. Experimental

The solar cells were fabricated on 5", pseudo-square silicon wafers. The wafers were chemically cleaned using saw damage removal (SDR) process and were given HF dip just before loading into the vacuum chamber to remove the oxide layer. The wafers were loaded in the vacuum system with base pressure of the order of 10-6 Torr with a minimum of 4 hours of system heating. Further, the wafers were also heated for half an hour before deposition to ensure consistent heating for all the runs. The electrode in the deposition chamber measured 1 'x 3' and the inter-electrode spacing was 13 mm. The variation in the RF power at 13.56 MHz was between 26 mW/ cm^2 to 33 mW/$cm^2$and pressure was varied from 600 mTorr to 700 mTorr. All the depositions were done at the heater temperature of 200° C which corresponded to the substrate temperature of 150° C, as confirmed by the temperature sensitive stickers. Also, the mass flow controllers (MFCs) were calibrated on absolute scale using displacement of water to ensure accurate flow values. p-tpye amorphous layer was deposited with 1% boron doping and n-type layer at the back was deposited with 3%

phosphene doped silane. Indium tin oxide layers on both sides were deposited pulsed DC sputtering.

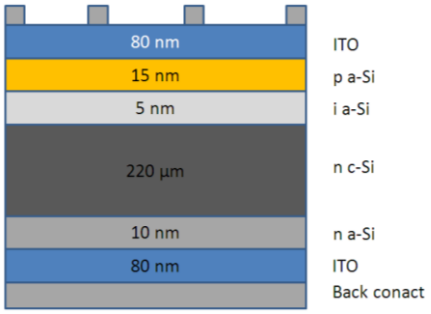

Fig. 1. The silicon heterojunction solar cell structure

The structure of the solar cell was as shown in Figure 1. The front side deposition was done before the rear side deposition and the wafer(s) was exposed to atmosphere once for flipping after front side deposition. The Indium tin oxide (ITO) deposition was done immediately after a-Si deposition without breaking the vacuum as the sputtering chamber is integrated with PECVD chamber in in-line fashion. All doped and undoped layers were deposited in one chamber only.

After layer depositions, the cells were screen printed using low-temperature curable paste. After the fabrication of complete solar cells, they were also annealed on the belt furnace used for curing the screen printed paste. Two different temperatures were used for annealing the cells. In one case, the annealing was carried out at 200 oC, whereas in the other case, the annealing was carried out at 220oC. In both the cases, the belt speed was same which subjected the wafers to the annealing temperatures for about 5 minutes.

The lifetime measurements were done on Sinton lifetime measurement setup without using any passivation solution.The cells are characterized by using I-V characteristics measured by I-V measurement setup. The I-V measurement set up has the provision to measure I-V characteristics of a solar cell in dark and under illumination. The solar cell to be tested is firmly held on a gold-plated, temperature controlled vacuum chuck and the measurement of current and voltage are made with 4-wire arrangement (2 wires for current and 2 separate wires for voltage). For all measurements under illumination, first the light intensity is checked and adjusted to 100 mW/ cm^2. Also, the temperature of the chuck is set at the desired temperature with tolerance of ±1 °C and monitored continuously using a PT100 probe inserted horizontally inside the gold plated chuck. Calibration of the intensity is performed with the help of the reference cell calibrated at NREL, USA (Make: PV Measurements Inc. USA, Model No.: PVM 230, 4 cm^2 area, Isc: 107 mA @ 25±0.2 °C, mounted on an Al block with BK7 glass protective window, with 4 wire contacts). The reference cell is certified for use to quantify or set the irradiance level of a light source used for testing solar cells and modules. When the short circuit current output of the reference cell is equal to its calibrated value of short circuit current, it indicates that the irradiance reaching the reference cell is equivalent to the irradiance (usually one sun) that was present during its calibration. The I-V measurement system comprises a controller module which interfaces with a power supply / electronic load on one hand and a PC on the other from where the parameters of measurements are set. The system operates with the help of embedded data acquisition and analysis software to sweep the forward light I-V characteristics.

3. Results and Analysis

The experiments were serially carried out to observe the effects of hydrogen dilution, silane depletion, annealing and chemical treatment. The effect of hydrogen dilution was studied on the intrinsic amorphous silicon layers as the minority carrier lifetime of the layers is a good indication of their passivation properties in the solar cell. A considerable difference was observed in the minority carrier lifetime of the layers after the annealing (Figure 2).

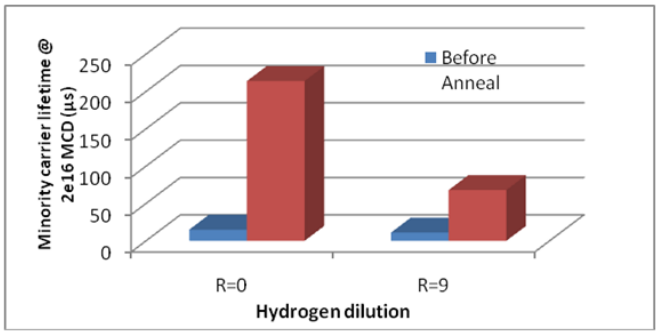

Fig. 2. The effect of annealing on the minority carrier lifetime of c-Si wafers embedded in intrinsic a-Si layers on two different hydrogen dilution where R = [H2]/ [SiH4].

Though the initial lifetime of the structure after a-Si deposition was similar to that of the wafer after saw damage removal (SDR) process, the lifetime improves considerably after annealing. It is attributable to the migration of hydrogen from the a-Si layer towards the interface and passivation of the dangling bonds [2]. It is conjectured that increasing hydrogen dilution did not incorporate additional loosely bound hydrogen that could passivate the interface by migration and that the character of film possible shifted towards nano-crystallinity. The lifetime of the annealed wafer improved from 50 µsec. to 200 µsec. as the hydrogen dilution in the intrinsic layer was reduced to zero. Henceforth, all the intrinsic layers in the device were deposited at zero hydrogen dilution.

Further, the effect of surface roughness and the silane depletion was studied together. Two different silane depletion factors were obtained by reducing the silane flow while keeping the process pressure constant. This increased the gas residence time and the cracking probability thereby increasing the silane depletion factor[4]. It has been observed that the effect of silane depletion is dependent upon the SDR time (Table 1). As the SDR time increased from 3 minutes to 4 minutes, the surface smoothness increased which could be recorded by visual inspection as well as by the increase in reflectivity.

Table 1. The average solar cell I-V characteristics at various saw damage removal (SDR) and total flow of i- and p-type a-Si layers. The ITO and n-type a-Si layer deposition conditions remained the same. All the values are averaged over two samples each.

SDR time (in min)	Gas flow	Voc (V)	Isc A)	Fill Factor	Aperture efficiency @ 138 cm^2(%)
4	f	0.608	4.09	0.71	13.0
	2/3*f	0.632	4.46	0.65	13.4
3	f	0.592	4.24	0.66	12.1
	2/3*f	0.601	4.51	0.65	13.2

It is obvious from the table that increasing SDR increased reflection and reduced the current and decreasing the total flow increased the open-circuit voltage. Also, the fill factor was reduced as gas flow was reduced. This could be because of non-uniform surface coverage because the layer depositions were done for the same amount time for both the flow values. This can be remedied in future by proportionately increasing the deposition time for low flow values. The highest efficiency achieved was 13.5% at a total gas flow value of 2/3th of flow for other process recipe for i- and p-type layers and SDR = 4 minutes (Figure 3).

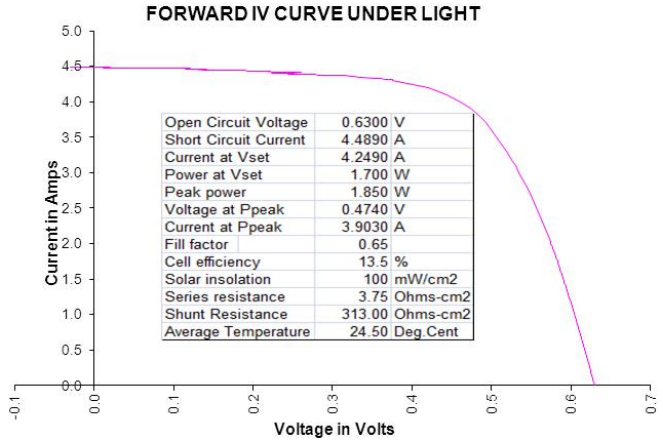

Fig. 3. The I-V characteristic of the solar cell obtained with SDR = 4 minutes and lower total gas flow values.

Having decided upon the silane depletion, SDR and the importance of annealing, the effects of rinsing and solar cell annealing were studied and complied as in Table 2. The effect of HF treatment on Si wafers has been well established [5, 6]. The role of DI water rinsing after the HF dip has been investigated here because rinsing with water for a few minutes can re-oxidize the H-terminated surface and bring down the device Voc, and lack of sufficient rinsing, on other hand, can contaminate the amorphous silicon film with fluorine. The upper limit of rinsing can be easily established by visual inspection. It was observed that rinsing for more than a couple of minutes turned the surface hydrophilic as it started retaining water droplets. To find out the importance of final rinse some of the wafers were given only a dip in the DI water after HF treatment while others were given 1 minute rinse in flowing water.

The average efficiency of six cells with 1 minute DI water rinse was 13.75% compared to average efficiency of 13.32% for cells with HF dip, before any annealing for both rinsing conditions. The gain in efficiency was due to improvement in short circuit current (Isc) and fill factor (FF), as shown in Table 2.

Table 2. The average values of cell parameters at various chemical and annealing conditions.

	DI water		Anneal	
	HF Dip	1 min. rinse	200 ˚C	220 ˚C
Isc (A)	4.72	4.764	4.636	4.747
Voc (V)	0.586	0.586	0.596	0.599
FF	0.66	0.68	0.706	0.716
Efficiency (%)	13.32	13.75	14.23	14.4

To observe the effect of annealing, half of samples from both 1 min. rinse and the single HF dip batch were combined together to form two batches with an average efficiency of 13.54% each. One batch was subjected to 200 ˚C anneal and the other was subjected to 220 ˚C anneal. The average results of both anneals on the samples are also shown in Table 2. It can be seen that 220 ˚C anneal produced better overall efficiency. The gain is achieved through the gain in fill factor and current suggested that anneal improves the amorphous layer and ITO properties. The gain in the mixed batch is not attributable to the passivation of junction by hydrogen migration.

Table 3. (a) The percent change in the cell parameters after annealing at 200 and 220 C. (b) The average absolute values of the cell parameter under different chemical and annealing conditions.

(a)	Average % change in cell parameters after annealing		
		HF Dip	1 min. rinse
200 C	Voc (V)	1.52	2.21
	Isc (A)	-1.74	-2.11
	FF	5.76	5.984
	eff. (%)	5.36	5.33
220 C	Voc (V)	1.19	1.96
	Isc (A)	-0.77	-0.19
	FF	5.71	6.70
	eff. (%)	6.39	9.96

(b)	Average cell parameters		
		HF Dip	1 min. rinse
200 C	Voc (V)	0.595	0.597
	Isc (A)	4.600	4.673
	FF	0.688	0.724
	eff. (%)	13.767	14.700
220 C	Voc (V)	0.599	0.600
	Isc (A)	4.740	4.755
	FF	0.704	0.727
	eff. (%)	13.667	15.133

Further, the effect of both annealing conditions on different rinsing conditions can be analyzed as shown in Table 3. The table summarizes the average absolute values of solar cell parameters as well as the percentage change experienced by the parameters after annealing. From the table, 1 min. rinse samples have higher efficiency for both the anneal conditions. Also, the individual parameters are higher for the 1 min. rinse samples. Interestingly, Voc values are almost identical for both the rinse conditions. So, the beneficial effect of 1min. rinse is in improved layer quality in terms of conductivity and transparency.

The percent change in the Voc, Isc and FF indicate that 1 min. rinse samples experienced greater improvement in Voc even though the final values are identical after annealing. This suggests that fluorine contamination hinders the surface passivation by hydrogen migration even though it may provide comparable passivation.

The reduced Isc and FF values with DI water dip suggest that the fluorine contamination of a-Si film is increasing the absorption in the film thereby degrading the quality of the layer. Further, annealing of the heterojunction structure has been linked to the migration of hydrogen atoms to the a-Si/c-Si interface and increase in the surface passivation and open circuit voltage. A comparison of the change in Voc for various rinse times showed that the Voc gain after annealing is greater for the samples that were rinsed for 1 min. For all annealing temperatures, there was an average gain of 2.1% in Voc for samples with 1 min. rinsing against 1.4% gain for sample with DI water dip. This suggests that fluorine contamination also affected the hydrogen migration in a-Si layer and passivation of the interface. The best results were obtained with annealing at higher temperature (220 C) and 1 minute rinse with DI water before loading the samples (Figure 4). The high efficiency was realised with high Voc and FF values as Isc remained low because of reflection from non-textured surfaces.

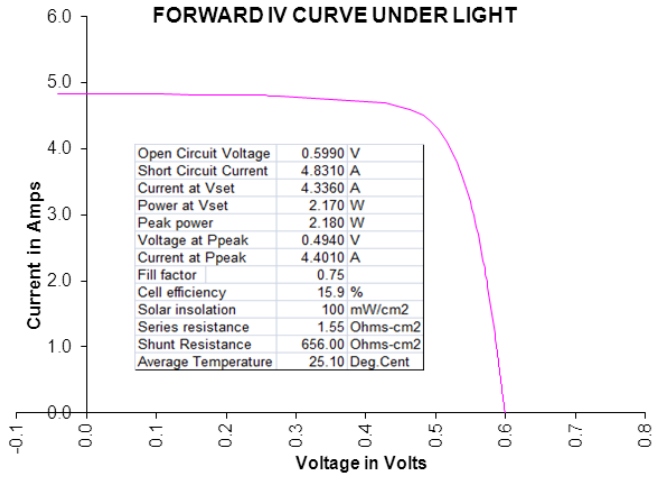

Fig. 4. The I-V characteristic of the solar cell with highest efficiency with annealing at 220 C and 1 minute final DI water rinsing. The average efficiency of the cells with same process conditions was 14.88%.

4. Conclusion

This article reports the effect of annealing, surface roughness, total gas flow andpre-deposition rinseon the efficiency of silicon heterojunction solar cells. The study established the beneficial effects of annealing both for the individual layer and for the solar cell. Also, it has been found that the smoother surface led to higher Voc but reduced the current appreciably because of the increase in reflection.

The positive effect of the silane depletion was also found dependent upon the surface smoothness. Nonetheless, increasing the silane depletion increased the cell efficiency for all SDR conditions. Hence, even though polished wafer is not desirable for heterojunction solar cell, the amorphous silicon deposition for heterojunction solar cells may be carried out with high silane depletion to achieve high open circuit voltage.

The effects of final rinsing with DI water and annealing were studied together for the performance of silicon heterojunction solar cells and it was found that if HF treated wafers are not rinsed thoroughly; fluorine contamination can harm the amorphous silicon film properties and affect cell performance. Most importantly, it also reduces the beneficial effects of annealing which has been found to improve the efficiency appreciably by increasing the junction passivation.

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