Prototype Development and Experimental Investigation on Cascaded Five-Level Inverter Based Active Filter for Large-Scale Grid-tied Photovoltaic

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Abstract- This paper presents a detailed laboratory prototype development procedure and realization of cascaded five-level inverter (CFLI) based shunt active power filter (SAPF) for large-scale grid-tied photovoltaic. A single-phase CFLI based SAPF is designed for mitigation of current harmonics and reactive power from medium- to high power distribution sector. Modified control theory for single-phase is used for execution of closed-loop control. Self-charging algorithm is used for DC-link voltage control. Phase-shifted pulse width modulation (PS-PWM) technique is used for generation of switching pulses for IGBTs. Driver circuits for IGBTs, sensor and amplification circuits have been designed in the Laboratory. System parameters are calculated as per required application. Snubber circuit is calculated for proper execution of inverter circuit. Control algorithm is executed in real-time controller dSPACE 1104. Finally, experimental results of single-phase CFLI are presented showing the effectiveness of proposed scheme in steady-state as well as in transient conditions.

Keywords Active Power Filter, Multilevel Inverter, dSPACE 1104, Grid-tied Photovoltaic**.**

1. Introduction

Power quality (PQ) is an emerging research area among engineers and other research personnel as number of renewable energy sources are integrated into current distribution sector. Large-scale grid-tied photovoltaic plays a major role in current energy scenario. But at the same instant it degrades PQ in several aspects. Degradation of PQ causes several adverse effects in current distribution scenario. Equipments used by consumers are main source of decrement in PQ. These end-user equipments including medium-voltage industrial drives are degrading PQ as they induce non-linearity into existing grid-tied system. At the same instant, this propagates through grid and deteriorates power factor and source current profile. Therefore, different devices like passive filters, active power filters (APF), distributed static compensators are projected in literature in order to counter these problems [1-4]. APF is found to be the most promising technology amongst all other technologies. Inverter circuit is the main part of shunt type APF unit but in case of industrial distribution line, it has limitations regarding selection of switching devices. Therefore, multilevel inverters (MLIs) are advantageous in this situation due to factors like small voltage and current rating of switches, no use of transformer, no filter circuits etc. Among available basic MLI topologies, cascaded inverter is one of the suitable MLI as this is modular in nature. Faulty portion can also be bypassed with relevant control algorithm [5-7].

Industries are using this topology in different purposes like non-conventional energy incorporation to MV induction motor drives. This topology needs least number of devices amongst all available MLIs. In case of filtering applications, no active power source is required. Separate capacitors need to be used with each H-Bridge. This modular structure offers transformer-less and cost-worthy solution to the industries in

case of high-power and medium to high-voltage applications [8, 9].

This topology can be easily used for higher voltage levels because of its modular structure. Many papers have been used this topology in recent past but a few literatures are focused on how to prepare the whole power electronic circuit based real-time system. M. Waware *et al.* has proposed MLI based SAPF for three-phase distribution sector. However, detailed hardware is not discussed [10]. S. Ray *et. al.* [11, 12] has proposed modified control algorithms for five-level cascaded inverter based active filter for three-phase and three-wire large-scale PV based grid-tied system. But, effectiveness of the proposed system is not tested in real-time conditions. Modified peak-detection based control algorithm is employed for five-level MLI based SAPF. This control algorithm is well capable to maintain unity power factor as well as maintain better voltage regulation [11]. However, this control algorithm performance degrades with non-ideal supply voltage condition. Therefore, single-phase synchronous reference frame (SRF) theory has been developed for overcoming this challenge. This control algorithm is able to perform well under non-ideal and unbalanced supply conditions [12]. These control algorithms [11, 12] are well tested in MATLAB/ Simulink but, practical validation of these control algorithms have not been tested yet. A new cascaded (CHB)-MLI structure is presented by Y. Suresh *et al.* [13], where, less number of dc-source and switching devices are used. This multi-cell structure is tested in both simulation and in real-time conditions. An advanced PWM technique has been used for even power distribution in case of transient conditions in [14]. This PWM can manage even power distribution among H-bridges in steady-state as well as load-changing conditions. M. Rajkumar *et al.* [15] presents a three-phase CHB-MLI based grid-tied inverter, where, MLI is used as an interfacing device between PV and grid. Perturb and observe MPPT method is used for tracking maximum power point. SVPWM technique is used for pulse generation for CHB-MLI. FPGA based platform has been used by authors for validating the control performance. In this context, N. Gupta *et al.* [16] presents CHB-MLI based SAPF structure which is able to provide active power to the grid in day light condition. This set-up works as reactive power compensator at night time. This structure also provides harmonic current mitigation which is generated from distribution sector. H. Liu et al. [17] presents one unique structure composed of two numbers of H-bridges and only one dc-source. In another H-bridge, only capacitor is used. This structure reduces the dc source requirement in case of active power feeding to the system. A. K. Panda *et al.* [18], [19] presents a modified structure for active power feeding capability which is composed of a single-dc-source and a single-phase transformer. Modified P-Q theory is used for reactive power management in [18]. This control is well capable of working in non-ideal supply conditions. Practical validation of this topology has been presented in [19] where, PSPWM technique is used for pulse generation where as i_d-i_q technique is used for active and reactive power control. S. Bacha et al. [20] shows single-phase seven-level CHB-MLI for grid-tied PV. Individual PV array and individual dc-link voltage control has been proposed in [20]. This system shows better efficiency with respect to others. A lot of research [21-30] is already carried in the area of SPAF and MLI based SAPF. However, detailed procedure to build this experimental set-up and performance testing of control algorithms in real-time conditions are still an issue.

Therefore, a five-level cascaded inverter based shunt active power filter is designed and developed in the laboratory. Step-by-step procedure of hardware built up is shown in this paper. Single-phase modified control algorithm is applied for closed-loop control performance of SAPF unit. Required voltage and current quantities are sensed using voltage and current sensors, respectively. Sensed voltage and current quantities are amplified according to the requirement of analog to digital (ADC) of dSPACE 1104. Closed-loop control algorithm is designed in MATLAB/ Simulink. Real-time workshop is used for generation of optimized C-code for real-time applications. Generated pulses are amplified and isolated with the help of driver circuit. Finally, performance of the proposed prototype is tested with diode-bridge rectifier based resistive-inductive loading.

Rest of the paper is designed as follows. Section two describes basic compensation principle of CFLI based SAPF. Section three shows proposed control algorithm. Section four depicts development of system hardware whereas Section five shows hardware results of proposed topology with non-linear loading conditions. Finally, an important decisive statement has been made in section 'six'.

2. Compensation Principle and System Architecture

In CFLI topology, each power electronic switch needs to block same amount of voltage but different voltage is being applied across capacitors in reverse blocking mode. Depending on switching combination, each device needs to block different voltage in different instant of time. Compared to Diode-Clamped MLI (DC-MLI), it requires more capacitors including dc-bus and auxiliary clamping capacitors. With different combination of clamping capacitors, it can produce same voltage level which gives redundancy in the circuit. As number of level goes high, bulky and costly power capacitors limit the use of it in industrial sector.

Output voltage level of CFLI is analogous to DC-MLI. In this topology (m-1) bus-capacitors are required for generating m level phase-voltage where as clamping-capacitors present in the circuit are (m-1) x (m-2)/2 per phase. Different levels of output voltage can be generated by selecting possible combinations of power electronic switches. Each phase is having an identical structure.

CFLI is a combination of single-phase H-Bridge cells, which can be linked in series behavior to produce higher level voltage output. CFLI based SAPF is applied for transformer less interconnection between APF unit and point of common coupling (PCC) of grid to overcome current related power quality problems in distribution sector. DC capacitors are integral part of CFLI based SAPF unit as an energy storage device and as a dc-voltage source which is required for reactive power compensation during transient and steady state. SAPF can generate current profile of equal magnitude and opposite polarity of load current with the help of appropriate control theory.

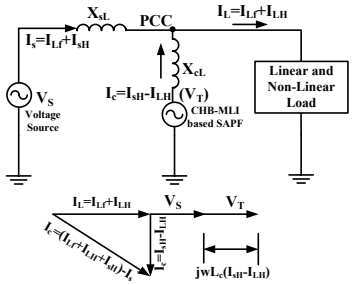


Fig. 1. Compensation Principle of CFLI based SAPF

The working principle of CFLI based SAPF is shown in Fig. 1 where instantaneous source current is equal to the summation of instantaneous load current and instantaneous compensating current as per Eq. 1.

$$i_s(t) = i_c(t) + i_L(t) = \left(i_{cp} + i_{Lp}\right)\sin(\omega t) \quad (1)$$

Where, sinusoidal voltage $v_s(t) = V_m \sin(\omega t)$ is taken as supply.

Non-linear loads draw current from source side which is summation of fundamental component and harmonic component of current, which can be expressed as per Eq. 2.

$$\left.\begin{aligned} i_L &= \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) = I_1 \sin(\omega t + \varphi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \\ &= I_1 \sin(\omega t)\cos(\varphi_1) + I_1 \cos(\omega t)\sin(\varphi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \end{aligned}\right\} \quad (2)$$

The instantaneous load power can be calculated as per Eq. 3.

$$\left.\begin{aligned} p_L(t) &= p_f(t) + p_r(t) + p_h(t) \\ &\text{or} \\ p_L &= v_s(t)\,x\, i_L(t) \\ p_L &= V_m \sin(\omega t)\left[\begin{aligned} &I_1 \sin(\omega t)\cos(\varphi_1) + \cos(\omega t)\sin(\varphi_1) + \\ &\sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \end{aligned}\right] \\ p_L &= V_m I_1 \sin^2(\omega t)\,x\cos(\varphi_1) + V_m I_1 \sin(\omega t)\,x\cos(\omega t)\,x\sin(\varphi_1) + V_m \sin(\omega t)\,x\sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \end{aligned}\right\} \quad (3)$$

Source is only liable for the active power flow between load and grid. Active power supplied by source can be calculated as per Eq. 4.

$$p_f(t) = V_m I_1 \sin^2(\omega t)\cos(\varphi_1) = V_m \sin(\omega t)\, x\, I_s \quad (4)$$

$$\begin{aligned} I_s &= p_f(t)/V_m \sin(\omega t) = I_1 x \sin(\omega t)\, x \cos(\varphi_1) \\ &= I_p x \sin(\omega t) \end{aligned} \quad (5)$$

SAPF will provide only reactive component and harmonics component of supply current in phase opposition. MLI based APF produces switching losses in real time operation along with some leakage losses. Therefore, utility needs to supply these additional components. Consequently, the peak value of source current after compensation is

$$i_{sp} = i_p + i_{s.loss} \quad (6)$$

where $i_{s.loss}$ is peak value of loss component. This source current is in phase with supply voltage as loss component of source current is shared by shunt APF and grid.

Harmonics generated by non-linear loads can be mitigated by controlling compensating current which is supplied by CFLI based SAPF whereas voltage stored in DC capacitors mainly supply loss components during switching action of MLI and supplies required energy during transient operation of SAPF. Fig. 2 shows CFLI based SAPF in block diagram manner with power circuit, driver circuit, sensors and amplification circuit.

3. Proposed Control Theory

Modified control system composed of three sections i.e. self-charging algorithm based DC voltage controller, enhanced PLL and PS-PWM. Enhanced PLL is used for harmonic and fundamental component extraction from polluted signal. It can also track frequency and phase with high accuracy. Finally PS-PWM is used to generate the required gate pulse for IGBTs of the converter. Modified control system for single-phase CFLI based power circuit is shown in Fig. 3.

DC voltage control is the first and foremost control aspect while considering CFLI based SAPF. Two DC capacitors are used for five-level CHB-MLI which supplies energy during transient condition. This modified control theory uses only one PI controller for controlling two DC voltages in case of five-level converter because tuning of more than one PI compensator increases the complexity of the control circuit. This principle can be extended successfully in case of high level inverters also. Precise DC voltage control during switching of load is required for this case so that one PI controller can be sufficient enough to take care of all DC-link voltages. Looking into this issue, self-charging algorithm is used as, it is having better transient performance with respect to normal PI controller based DC voltage control which is used here for 5-level CFLI based filtering application. Bode-plot based method proposed by B. A. Angelico *et al.* [21] is used in this paper for tuning proportional and integration constants of PI compensator. Energy conversion principle is used in self-charging algorithm for charging and discharging of DC-link capacitors. At the starting of the SAPF system, an additional energy is required to regulate dc-link voltage from the utility for charging the capacitors. Throughout the charging procedure, capacitor voltage has little fluctuation nearer to the desired DC-link voltage. This phenomenon provides

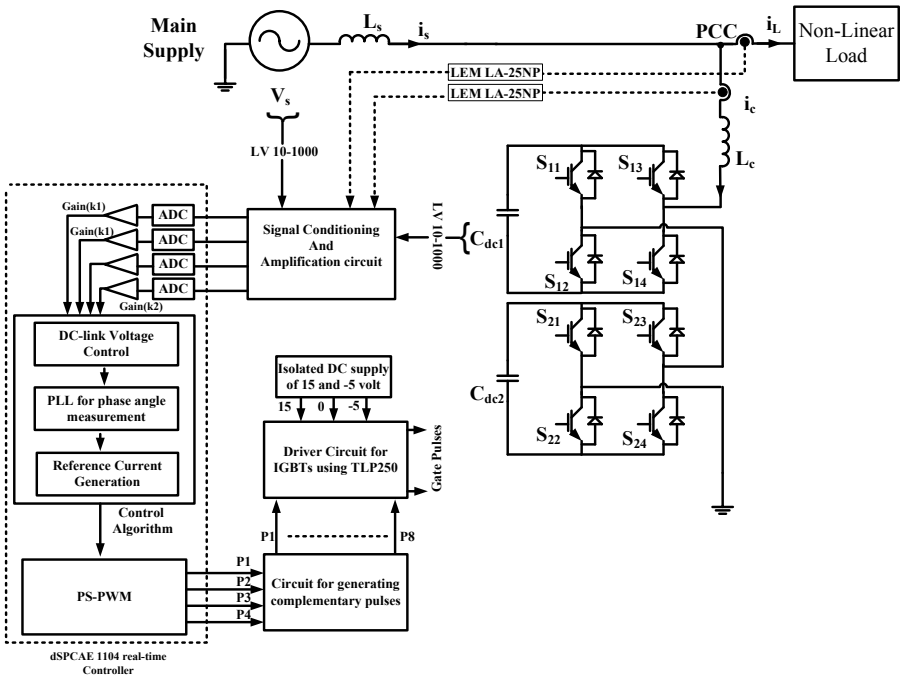


Fig. 2. Schematic Diagram of single-phase CFLI based SAPF

some amount of energy change in the dc-link. The amount of energy stored in the capacitor is denoted by:

$$\Delta E = C/2\,.\,[(V_{dc}^*)^2 - (V_{dc})^2] \quad (7)$$

At the same time, the energy delivered by utility for the capacitor is represented by Eq. 8.

$$E_{ac} = P.\,t_C = V_{RMS}I_{RMS}t_C \quad (8)$$

As capacitor takes one half-cycle to charge itself so, t_c can be considered as T/2, where T can be defined as per supply frequency 50 Hz. Again, V_{RMS} and I_{RMS} can be expressed in terms of peak magnitudes as described by Eq. 9.

$$E_{ac} = V/\sqrt{2}\,.\,I_{dc}/\sqrt{2}\,.\,T/2 \quad (9)$$

As per energy conversion principle, by neglecting switching losses of CFLI based VSI, change in energy is denoted by

$$\Delta E = E_{ac} \quad (10)$$

So, from Eq. (8) and Eq. (10), $C/2\,.\,[(V_{dc}^*)^2 - (V_{dc})^2] = (V.\,I_{dc}.\,T)/4$

So, I_{dc} can be defined as per Eq. (11)

$$I_{dc} = (2C/VT).\,[(V_{dc}^*)^2 - (V_{dc})^2] \quad (11)$$

In self-charging algorithm, voltage error 'e' can be defined as per Eq. 12. Voltage error is minimized through PI compensator.

$$e = [(V_{dc}^*)^2 - (V_{dc})^2] \quad (12)$$

Self-charging algorithm is having a simple construction of DC voltage control in case of CFLI based SAPF. This algorithm exhibits good transient response of DC-link voltages with respect to PI controller based approach. Above mentioned simple calculative effort is only needed for the generation of reference signal.

Finally, reference current generated with the help of self-charging algorithm and PLL is compared with sensed compensating current signal and error is passed through a AC-PI controller and consequently this reference signal is compared with phase-shifted triangular carrier waveform of 2KHz. PS-PWM technique is used for generation of required gate pulses for CFLI circuit in order to compensate non-linear load current present in MV distribution sector.

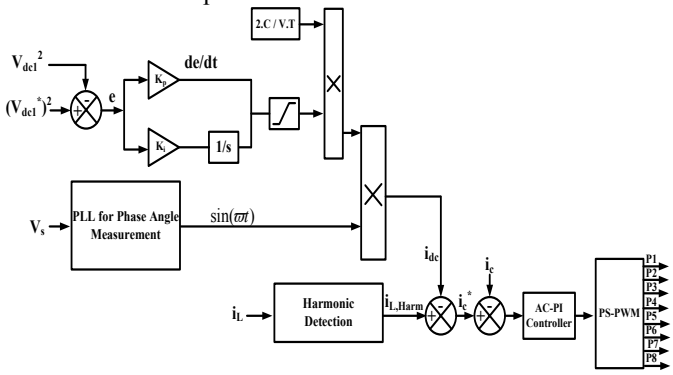


Fig. 3. Proposed Control Algorithm of Single-Phase CFLI based SAPF

4. Development of System Hardware

The system hardware prototype of CFLI based SAPF is discussed in this section. Any power circuit requires some additional driver circuits to drive the semiconductor switches, signal conditioning, measuring of various parameters etc. In this section, all the general purpose driver circuits are discussed in detail. Each circuit is tested in various possible conditions. These circuits are applied on power circuits.

DSP of dSPACE 1104 control card is used to implement the control scheme and generate the required gate pulses. The control card is composed of master PPC and slave PPC. Master PPC provides 4 analog inputs with 16-bit resolution and other 4 analog inputs with 12-bit resolution. The control card also provides 8 digital to analog pins with 16-bit resolution. It is also having 20 digital input output (IOs) pins. Slave PPC is having 1 number of 3 phase PWM pins and 4 numbers of single-phase PWM pins. This also has 14 number of digital I/O channels. DSP TMS320F240 is used for

programming in DS1104 unit. This dSPACE is connected to one host PC. Host PC is having intel (R) core (TM) i7-6700 CPU @ 3.4 GHz, 4 GB RAM, 64-bit operating system. X64 based processor with Microsoft windows operating system and Control-Desk 3.7.3. MATLAB software, hardware configuration of MATLAB/ Simulink is used for the programming and implementing the proposed control scheme.

4.1. Development of System Hardware of CFLI Circuit

As discussed in section 2, CFLI circuit consists of eight semiconductor switches. These switches should have self-commutating property; hence IGBTs, MOSFETs or GTOs are the best candidate for it. The four switches are connected in single phase bridge form. This 'H' shaped bridge connection is connected in cascaded manner. Each switch should have anti-parallel diodes. These diodes can be in-built in the semiconductor device or can be connected from outside the switch. An electrolytic DC capacitor needs to be connected between positive and negative rail of one 'H' bridge. At the same time, snubber circuit also needs to be used for dv/dt protection to the circuit.

4.1.1. Selection of Semiconductor Switch

Selection of semiconductor switch in an electrical circuit depends upon various parameters like v-i characteristics of the device, switching frequency, electrical stress rating, thermal stress rating etc. Voltage and current withstand capability and switching frequency are the most important factors in the selection of a semiconductor switch. SCRs are available with high current and voltage rating but can operate at low frequencies only. Another problem with SCR is that, it requires external commutation circuit. On the other hand IGBTs, MOSFETs and GTOs are self-commutating devices. They can operate at high frequencies. MOSFET can operate at a frequency up to 100 kHz but voltage and current rating is lower than the IGBTs. For medium frequency range of 20 kHz, IGBTs can be used. They are available in high current and voltage rating. CFLI operates at 2 KHz switching frequency. Although thyristor is already available with higher voltage and current rating, but the switch used in CFLI must have self-commutating property hence SCR cannot be used for this operation. High rating IGBTs can be used for the operation of proposed circuit. ST make GW30NC120HD is used as IGBT of required rating.

4.1.2. Snubber Circuit Design

During transient conditions, voltage across the device can exceed the maximum limit which can damage the switch as well as complete circuit. Therefore, limiting the transient voltage within permissible range is very important factor from the protection point of view. The snubber circuit provides a short term alternative path around the current switching device so that inductive element may discharge safely.

A small resistance with capacitor in series can be used as a RC snubber circuit. Fig. 4 shows IGBT connected with snubber protection circuit. When a sudden voltage is appeared across the switch, dv/dt triggering may occur. With the presence of the snubber circuit, capacitor behaves as short circuit for an instant of high voltage appearance and the voltage across the device become zero. Then, capacitor charges slowly. During the discharging operation of the snubber capacitance, the impedance of the circuit is quite low causing high discharging current. So, a small resistance is used to limit the discharging current of the capacitor.

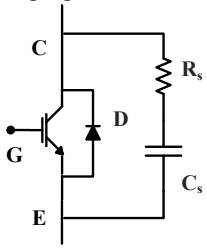


Fig. 4. Snubber circuit with IGBT

A single-phase 'H-bridge' is designed in the laboratory and this is built in Printed Circuit Board (PCB). The connection diagram of 'H-Bridge' is shown in Fig. 5.

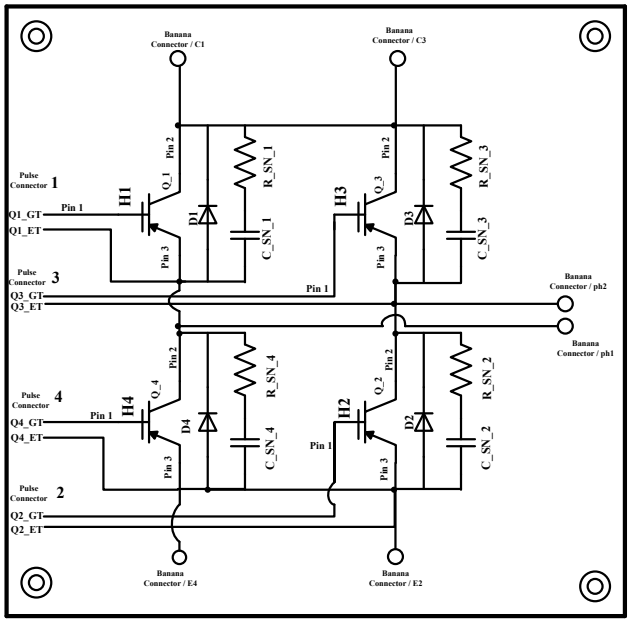


Fig. 5. H-bridge circuit model

4.2. Development of Gate Driver Circuit

Gate driver circuit is required in between the real-time controller and the semiconductor switches in power circuit. The purpose of the gate driver circuit is to amplify the pulse generated from the dSAPCE1104 controller. This also provides electrical isolation between control circuit and power circuit, dynamic short circuit protection by using dead band between two switches to the same leg. Various opto-isolator ICs like MCT2E, TLP250, TLP350 etc. are available as isolation between power and control circuit.

4.2.1. Pulse Amplification and Isolation Circuit

The semiconductor devices like MOSFETs require a gate pulse of +12V to trigger the switch, whereas IGBTs require a gate pulse of +15V to turn the switch on and -5 V to turn the switch off. The digital output of the dSPACE 1104 controller is in the order of 0 - 5V. Hence, the voltage level generated by the real-time controller is not sufficient for switching ON the semiconductor switches (IGBTs). The gate

driver circuit consists of two parts i.e. isolation and pulse amplification. Opto-coupler IC is normally used to amplify the pulse generated by the controller to the level required by the semiconductor switches.

Though DS1104 is user-friendly, but this controller is costly. The current flow in the controller circuit is generally in the rage of 0.2 – 0.5 A, whereas the current level in the power circuit can be high as 10 A – 2 kA. Hence, DSP controller needs to be electrically isolated from the power circuit. Among all available opto-coupler ICs, TLP250 is chosen as TLP250 is cost-effective and this TLP can work well in the frequency range of 1 kHz to 10 kHz.

TLP250 is Toshiba make 8 pin DIP package IC. TLP250 can give the gate pulse of 10 - 35V at the output. It provides isolation between power circuit and controller circuit up to 2500V. TLP250 is suitable for the laboratory prototype for moderate voltage level and 25 kHz switching frequency. The internal architecture with schematic diagram for pulse amplification circuit using TLP250 is shown in Fig. 6.

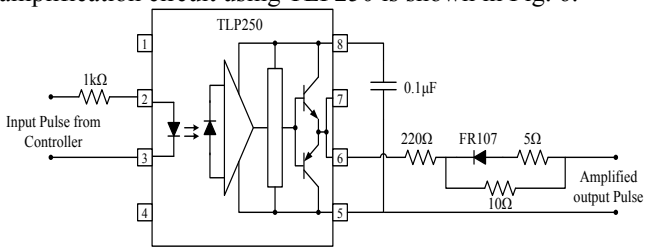


Fig. 6. TLP based gate pulse amplification and isolation circuit

As shown in the Fig. 6, input pulse from the real-time controller is given between pin number 2 and 3. Pin number 1 and 4 are not connected. 1 kΩ resistance is used at the input of the opto-coupler to limit the current from controller. At the output side, supply is connected between pin number 5 and 8. The voltage level of the supply connected to the TLP is exactly same as the level required to trigger the semiconductor devices i.e. +15V, -5V for IGBTs and +12V, 0V for the MOSFETs. However, this voltage level may be varied according to datasheet of power semiconductor switch. A ceramic capacitor of 0.1μF should be connected from pin number 5 to 8 to stabilize the operation of the high gain amplifier. The output of TLP250 can be taken from pin number 6 or 7. Both the pins are shorted internally. The ground of the output pulse can be taken from pin number 5. The circuit at the output terminal (pin number 6) consists of fast recovery diode FR107, ON resistance of 10 Ω and OFF resistance of 5Ω. This circuit is mainly designed for IGBT's gate pulse. Fig. 7 shows the amplification of 5 V input pulse to +15 V to -5 V amplified pulse through the opto-coupler circuit. Ground terminal of amplified gate pulses need to be electrically isolated. This isolation is made by using step-down transformer (230V to 15-0-15V, 500 mA). Separate transformers are used for each gate driver circuit. After stepping down of AC voltage, diode-bridge uncontrolled rectifier is used for generating DC voltage. This DC voltage is stabilized by using two capacitors in series manner. Positive (7815) and negative (7905) voltage regulators are used for generating constant DC voltage of +15V and -5V with respect to ground terminal of transformer secondary. Normally, a high value of resistance needs to be connected in between gate and emitter terminal of IGBT. High value resistance of 18 k, ¼ Watt is attached in between gate and emitter terminal of IGBT for this driver circuit.

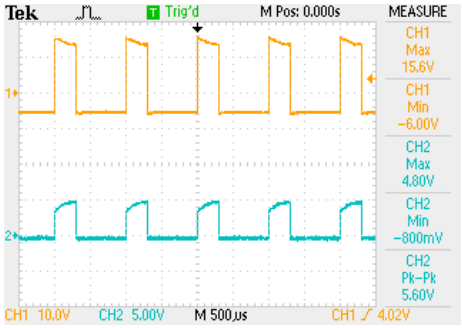


Fig. 7. Hardware results of gate driver amplification and isolation circuit

4.2.2. *Dead Band Circuit*

Two complimentary gate pulses are given to the two semiconductor switches of the same leg of the bridge. Ideally, the switch should turn - ON and turn – OFF instantly. But, practically it takes some time to turn ON or OFF which is called as switching time. When one of the switches is getting turn ON then other should turn off completely. If both the switches are switched ON at the same instant then there may be a short-circuit condition. During this interval of time there may be a chance that the both switches start conducting and short circuit the complete leg. It can short the supply or load and may cause for the fault in the circuit. At the same time, every IC and other semiconductor devices need some minor time to respond. But, as the switching frequency is high enough, some delay need to be provided as a precaution of short-circuit condition between two-switches of one leg.

The concept of dead band is one of the best solutions available for this problem. If the pulse of one switch is delayed for a short period of time during rising edge, then the other switch can turn OFF completely. Hence, this problem may be rectified. The schematic diagram of the dead band circuit is shown in Fig. 8. It consists of RC circuit to delay the switching ON instant of the pulse.

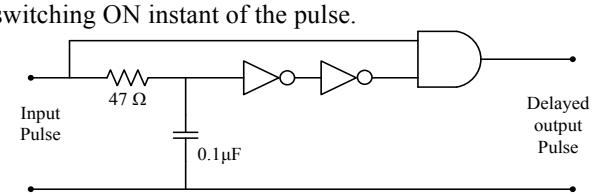


Fig. 8. Circuit diagram of dead band circuitry

The proposed TLP250 based gate driver circuit with dead band is fabricated in the laboratory to test the effectiveness of the circuit. AND gate IC 7408 and NOT gate IC 7404 is used to fabricate the dead band circuit. Combination of resistance and capacitance decide the amount of dead band required in the circuit. The hardware results of the dead band circuit are given in Fig. 9. Fig. 9 shows 3 μs dead-band is given between input of opto-isolator and output of opto-isolator. A dedicated driver circuit is designed for two IGBTs where pulse amplification as well as electrical isolation is maintained. At the same time, this driver circuit is able to provide short circuit protection in the help of dead-band circuit. The detailed design of driver circuit is shown in Fig. 10.

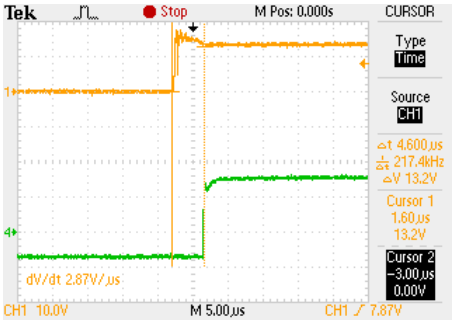


Fig.9. Hardware result of dead band circuit

This paper shows driver circuit designed for two numbers of IGBTs in one leg. Resistance and capacitance combination with 7404 and 7408 IC provides required proper dead-band operation. TLP250 provides amplification as well as isolation. Dedicated DC supplies are also a part of this driver circuit as DC supply of 5V is needed for driving ICs 7404 and 7408. TLP250 requires +15 V and -5V at pin number 8 and 5, respectively. These drive ICs require isolation which is done by using different transformers. On and off resistances on the output side of TLP 250 are also provided.

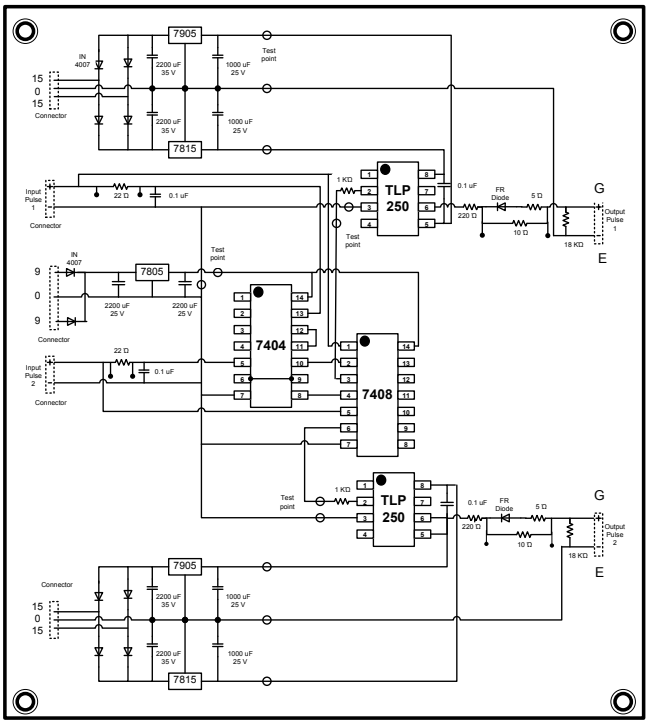


Fig. 10. Driver circuit for two IGBTs of one leg of Inverter Circuit

4.3. Signal Conditioning Board for System Parameter

Measurement of various system parameters like supply voltage, load voltage, supply- and load- current, DC link voltage and their conditioning is required for accurate, reliable and effective control operation. High accuracy, easy installation, linear and fast response are the necessary and important parameter for the measurement circuit. Use of multi-range hall-effect transducers can fulfil these requirements to a great extent. Any control algorithm needs number of voltage and current signals from the circuit. This section describes the different signal conditioning circuit for the implementation of the proposed control algorithm.

4.3.1. Current Sensor Circuit

The current sensors are required to sense the current in the various part of the circuit and generate a proportional signal to the DSP controller in its range. The LEM make hall-effect current transducer type LA 25-NP is used. The main advantages of LA 25-NP are high accuracy, good linearity, optimized response time, no insertion losses, low temperature drift and current overload capability. This current transducer requires ±12V to ±15V DC supply voltage to operate. It is having primary nominal rms current rating of 25A and can measure 0 to ±25A at the primary side. LA 25NP can be used for the measuring of AC and DC current of the circuit. This current transducer provides galvanic isolation between high voltage primary circuits to the secondary side electronic level low voltage circuit. The circuitry to get the output voltage proportional to the input current is shown in the Fig. 11.

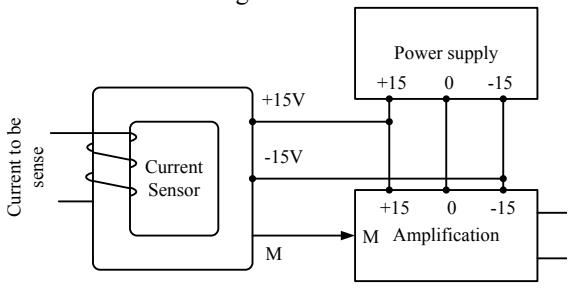


Fig. 11. Circuit configuration of current sensor circuit with amplification

4.3.2. Voltage Sensor Circuit

Generation of desired gate pulse for semiconductor switches require a closed loop control algorithm. Generally, the entire control algorithm depends upon the voltages of various parts of the circuit. Hence, instantaneous voltage

measurement or sensing in various parts of the circuit is required. Since the voltage level of the power circuit is high and cannot give to the DSP controller directly, so it is needed to be step down proportionally. The voltage signal can be sensed by a simple combination of resistances by forming a voltage divider circuit. However, measuring and stepping down the voltage by this method has various problems. In this method the voltages dropped across the resistance causes high level heating. Since number of voltage sensors in the circuit can be high, it causes more energy losses and makes the system less efficient. On the other hand this method of voltage sensing does not have any electrical isolation between high voltage power circuit and low voltage controlling circuit. Hence, any disturbance in power circuits, noise or any fault can pass to the control circuit directly and may damage or disturb the control circuit.

Keeping all this conditions in view, hall-effect voltage sensors are preferable for voltage measurement. In this paper, LEM make LV 25-1000 voltage transducer is used for measuring the voltages at different point of the circuit. LV 25-1000 having many advantages like high accuracy, very good linearity, low response time, low disturbance in common mode, high immunity to external interference and low thermal drift. It has ingrained galvanic isolation between high voltage power circuit and electronic level low voltage control circuit. This transducer required ±12V to ±15V DC supply to operate. LV 25-1000 can measure DC/AC voltage of level up to 1500V on primary side.

Two terminals named as +HV and –HV need to be connected in the circuit where voltage measurement is required. The output voltage from the sensor can be taken from the terminal M. Fig. 12 shows the circuitry of LV 25-1000.

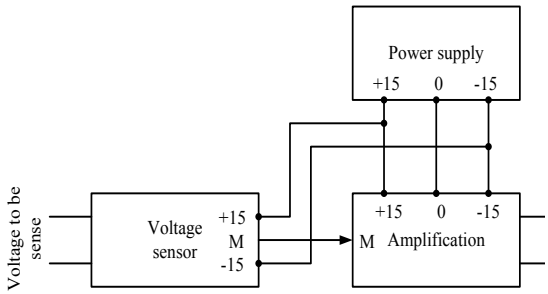


Fig. 12. Voltage sensing circuit with amplification

4.3.3. *Sensor Amplification Circuit*

The voltage signal at the output of current and voltage transducer can be higher than 3.3V depending upon the various parameters like, measured input voltage or current, type of transducer and the method of using the transducer (more number of turns may wound in case of current transducer). The analog to digital converters (ADCs) of most of DSP controller have the voltage limit of 3.3V. The higher voltage can damage the complete controller. Hence, surety of maximum voltage from the transducers is essential for the protection of DSP controller.

Sensor amplification circuit as shown in Fig. 13 can be used to control the output voltage of the transducers. It consists of three cascaded op-amp circuits. TL081 op-amp ICs are used in this model. Each IC requires ±15V to operate. The purpose of first and third op-amps circuits acts as a buffer to the circuit whereas the second one is used for scaling the output of the amplification circuit. The output of the transducer is given to the 3rd terminal of the first op-amp and the scaled output can be taken from the 6th terminal of the 3rd op-amp based buffer circuit. A 10 kΩ variable resistance is used for the negative feedback of scaling circuit. This variable resistance decides the amplification of the input signal of the circuit. The value of the variable resistance is set such that the output of the amplification circuit should not exceed 3.3 V for the maximum voltage level of the power circuit. Once the scaling parameter is done, amplification factor should be calculated by measuring input and output voltages of the amplification circuit and different source voltage and current level. The calculation of amplification factor is required to provide the same amount of gain inside the controller.

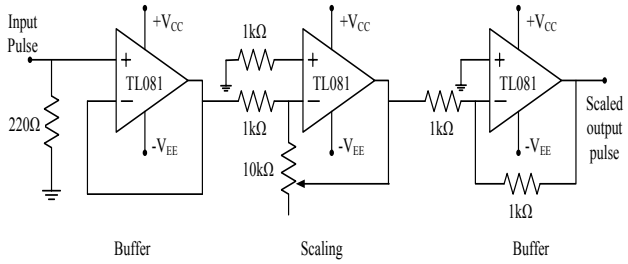
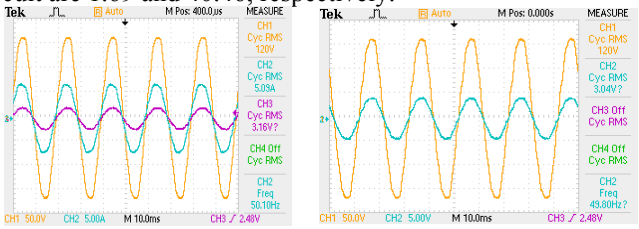


Fig. 13. Signal amplification circuit

Fig. 14 (a) shows the amplification circuit results with current sensing circuit whereas Fig. 14 (b) shows the amplification circuit results with voltage sensing circuit. The calculated amplification factor of current and voltage sensing circuit are 1.69 and 40.46, respectively.



(a) (b)

Fig. 14.Hardware results of (a) Current amplification circuit and (b) Voltage amplification circuit

4.4. *Design of Non-linear Loading*

In electrical networks and distribution networks, current-type and voltage-type of non-linear loads are major sources of poor power quality by deviating current wave shape into non-sinusoidal one. Diode-bridge rectifiers with resistive-inductive and resistive-capacitive loading on consumer side are commonly used as non-linear loads for real-time realization. Therefore, a diode-bridge rectifier is built in laboratory by using 16KSR power diode. Terminals of input and output are connected externally for the rest of the circuit connections. The whole module is mounted in a heat-sink module as proper heat-dissipation is necessary for proper operation of diode-bridge rectifier.

4.5. *Control Algorithm Deployment using dSPACE 1104*

DSP of dSAPCE 1104 control card is used to implement the control scheme and generate the required gate pulses. The control card is composed of master PPC and slave PPC. Master PPC is having 4 analog inputs with 16-bit resolution

and other 4 analog inputs with 12-bit resolution. The control card also provides 8 digital to analog pins with 16-bit resolution. It is also having 20 digital input output (IOs) pins. Slave PPC is having 1 number of 3 phase PWM pins and 4 numbers of single-phase PWM pins. This also has 14 numbers of digital I/O channels. DSP TMS320F240 is used for programming in DS1104 unit. This dSPACE is connected to one host PC. Host PC is having intel (R) core (TM) i7-6700 CPU @ 3.4 GHz, 4 GB RAM, 64-bit operating system. X64 based processor with Microsoft windows operating system and Control-Desk 3.7.3. MATLAB software, hardware configuration of MATLAB/ Simulink is used for programming and implementation of the proposed control scheme.

SIMULINK of MATLAB add-on software that enables block diagram based modeling and analysis of linear, nonlinear, discrete, continuous and hybrid systems. Real-time workshop (RTW) is an efficient platform for optimized code source generation. This can be executed on PC, microcontrollers, signal processors etc. Real-time interface by add-on software of dSPACE provides block libraries for I/O hardware integration of dS1104 R & D controller board and optimized code generation for master and slave processors of the board. dSPACE's control desk is a software tool interfacing with real-time experiment and provides easy and flexible analysis, visualization, data acquisition and automation of the experiment.

The optimized code is automatically generated by RTW of MATLAB in conjunction with RTI of dSPACE. The dSPACE of real-time interface is used to build, download and execute the generated code on the dSPACE 1104 board to obtain signals at CP1104 connector panel. Output signals or any variables in the model can be observed or stored in the control desk. Twelve number of master bit I/Os are configured for outputting the twelve gating signals to isolation board where these are also complimented and through driver circuit given to IGBTs in the CFLI. Fig. shows the schematic of dSPACE (DS1104) board interfaced with the host PC and real-world plant.

5. Simulation and Experimental Results

A five-level CFLI based SAPF is simulated in MATLAB/simulink for 6.6 kV source voltage. Uncontrolled bridge rectifier based R-L and R-C loading is used as non-linear loads present in distribution sector. Fig. 15 (a)-(c) shows performance of CFLI based SAPF unit in both steady-state as well as in transient conditions with R-L based non-linear loading. Fig. 15 (a) shows steady-state performance of SAPF unit in terms of source voltage (V_S), source current (I_S), load current (I_L), compensating current (I_C) and dc-link voltage (V_{dc1}). Fig. 15(b) shows transient performance of SAPF unit when load is increasing whereas Fig. 15(c) shows transient response of SAPF unit when load is decreasing in a step manner. It has been observed that, in both the cases system attains steady-state after sustaining transient condition. Fig. 15(d) shows THD profile of I_S after compensation of non-linear current waveform.

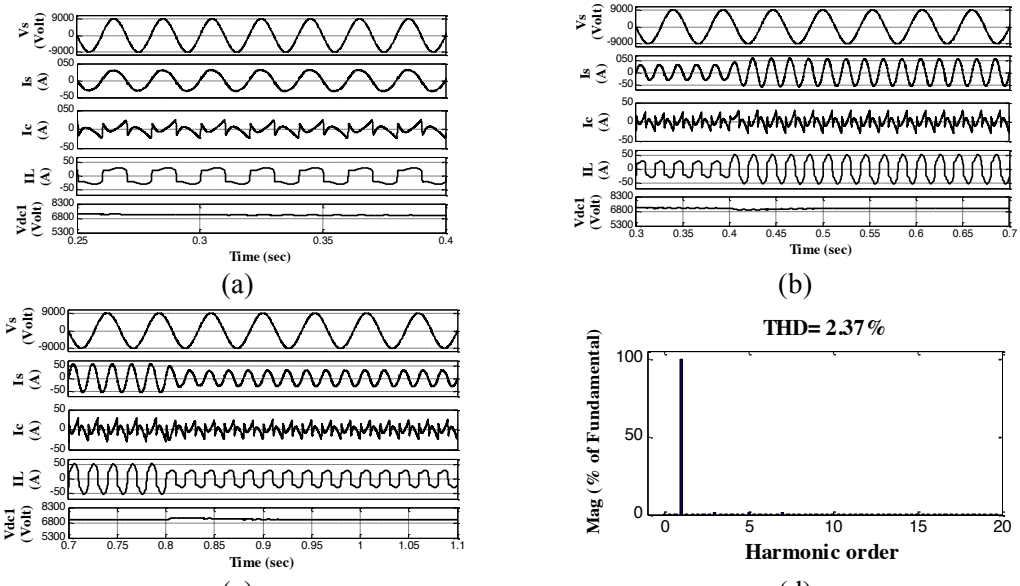


Fig. 15. (a)Steady-state performance of CFLI based SAPF with R-L loading (b) V_S, I_S, I_L, I_C waveform while increasing loading (c) V_S, I_S, I_L, I_C waveform while decreasing loading (d) THD of I_S after compensation

System is also simulated with uncontrolled bridge rectifier and R-C loading. Fig. 16 (a)-(c) shows performance of CFLI based SAPF unit in both steady-state as well as in transient conditions with R-C based non-linear loading. Fig. 16 (a) shows steady-state performance of SAPF unit in terms of V_S, I_S, I_L, I_C and V_{dc1}. Fig. 16(b) shows transient performance of SAPF unit when load is increasing whereas Fig. 16(c) shows transient response of SAPF unit when load is decreasing in a step manner. It has been observed that, in both the cases system attains steady-state after sustaining transient condition. Fig. 16(d) shows THD profile of I_S after compensation of non-linear current waveform due to the effect of R-C based non-linear loading.

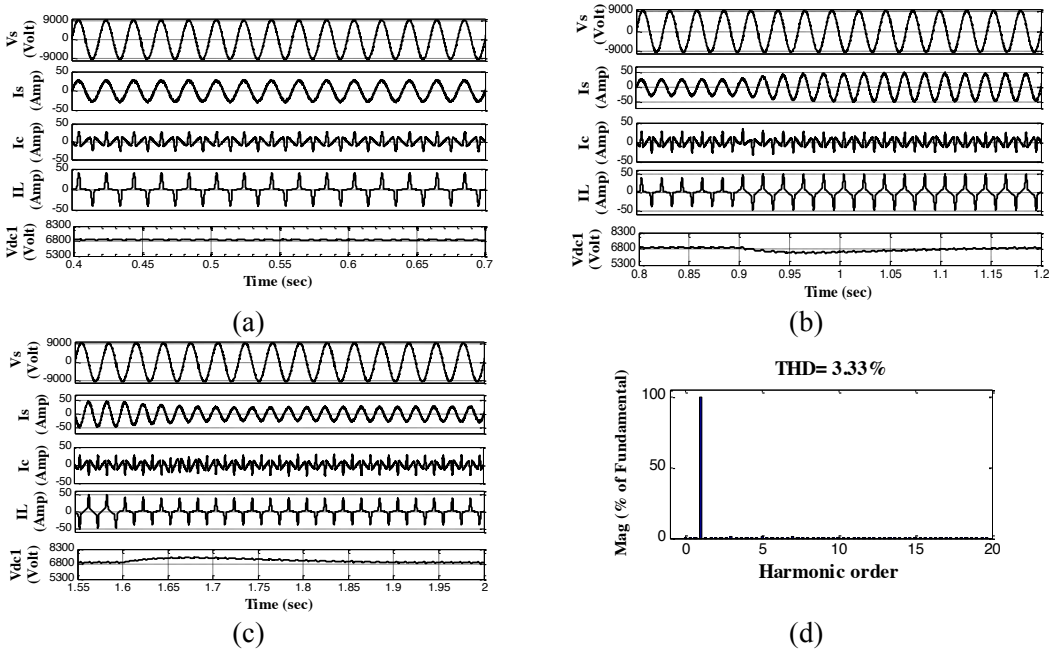


Fig. 16. (a)Steady-state performance of CFLI based SAPF with R-C loading (b) V_S, I_S, I_L, I_C waveform while increasing loading (c) V_S, I_S, I_L, I_C waveform while decreasing loading (d) THD of I_S after compensation

A prototype model of single-phase CFLI based SAPF is developed in laboratory condition. This is done by integrating CFLI based power circuit, gate driver circuit, dead-band circuit, pulse amplification circuit, and signal conditioning circuit. Non-linear load is designed and fabricated in the laboratory. The proposed control algorithm is designed in real-time controller dSPACE 1104. PS-PWM is used for switching of IGBTs in inverter circuit. The complete set-up used for experimentation is shown in Appendix.

Proposed circuit is tested with non-linear loading conditions including diode-bridge rectifier and R-L loading. Tektronix make TPS 2014B and power quality analyzer Fluke made 43B is used to capture the required waveform. Steady-state results have been presented in Fig. 17(a) - (d). Fig. 17(a) shows non-linear I_S with sinusoidal V_S. Fig. 17(b) shows THD profile of I_S which is 32.8 %. Fig. 17(c) shows steady-state performance of proposed system. V_S, I_S, I_C, I_L are shown in Fig. 17(c). I_S becomes sinusoidal even though I_L is non-sinusoidal. Fig. 15(d) shows THD profile of I_S after compensation of harmonic component. Source current THD is maintained according to IEEE imposed limits.

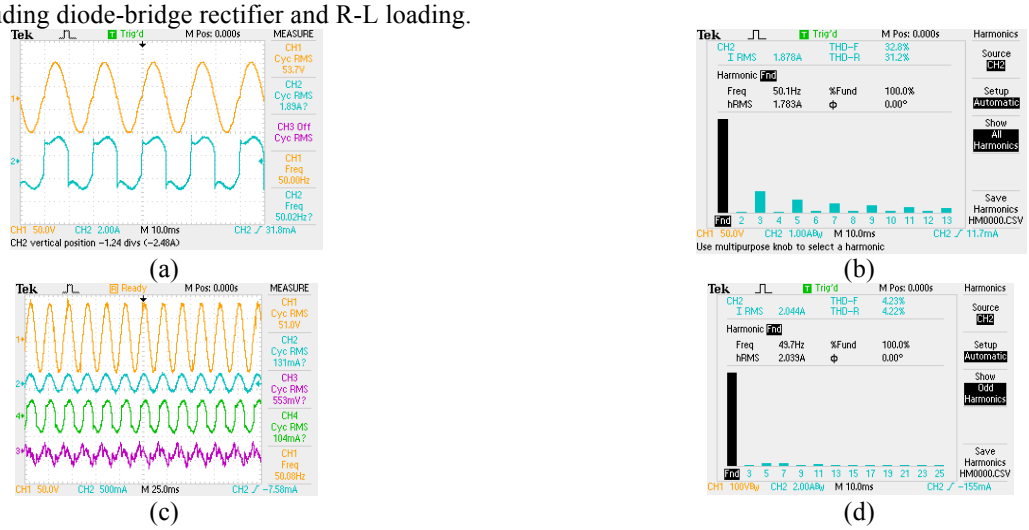


Fig. 17. Steady-state performance of CFLI based SAPF (a) V_S with non-linear I_S (b) THD of I_S before compensation (c) V_S, I_S, I_L, I_C steady-state waveform (d) THD of I_S after compensation

Proposed circuit is also tested with non-linear loading conditions including diode-bridge rectifier and R-C loading. Steady-state results of CFLI based SAPF have been presented in Fig. 18(a) - (e). Fig. 18(a) shows non-linear I_S with sinusoidal source voltage V_S due to loading whereas Fig. 18(b) shows THD profile of I_S which is 74.5 %. Fig. 18(c) shows steady-state performance of proposed CFLI based SAPF system after integration of SAPF unit with grid at PCC. Various waveforms (V_S, I_S, I_C, I_L) are shown in Fig. 18(c). I_S becomes sinusoidal even though I_L is non-sinusoidal. Power factor also becomes almost unity. Fig. 18(d) shows THD profile of I_S after compensation of harmonic component. Fig. 18(e) shows five-level voltage generated by CFLI along with the operation of SAPF. Source current THD

is maintained according to IEEE imposed limits in both the cases.

6. Conclusion

A detailed laboratory prototype development procedure and realization of cascaded five-level inverter based shunt active power filter for large-scale grid-tied PV is proposed in this article. A single-phase CFLI based SAPF is designed for mitigation of current harmonic component and reactive power from medium- to high power solar-PV based distribution sector. Self-charging algorithm is used for DC-link voltage control in case of CFLI based SAPF. Detailed pulse amplification circuit, isolation circuit for gate driver, dead-band circuit, signal measurement and amplification circuit are designed in laboratory. Detailed step-by-step procedure is shown in figure. Snubber circuit is designed for proper execution of inverter circuit. The proposed control algorithm is executed in real-time controller dSPACE 1104. Finally, experimental results of single-phase CFLI are presented for showing the effectiveness of proposed scheme under non-linear loading conditions.

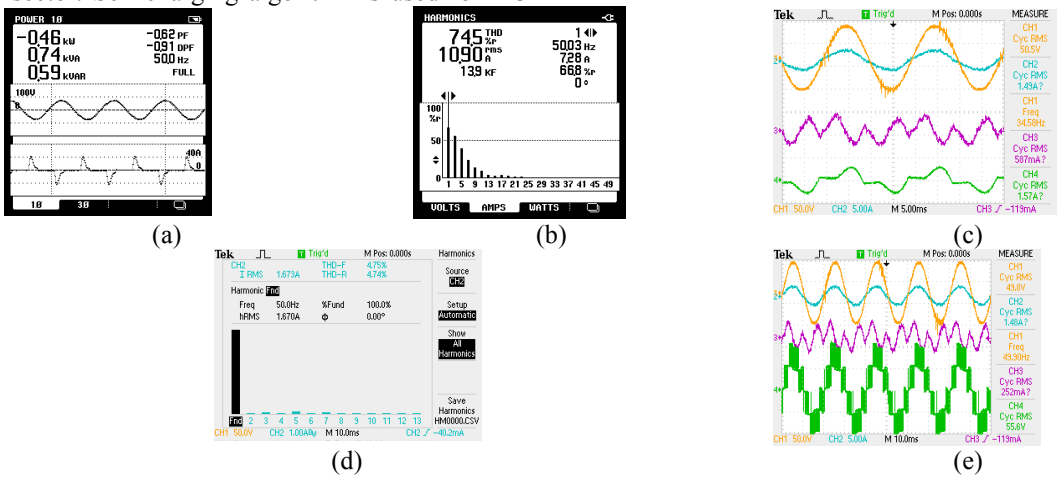
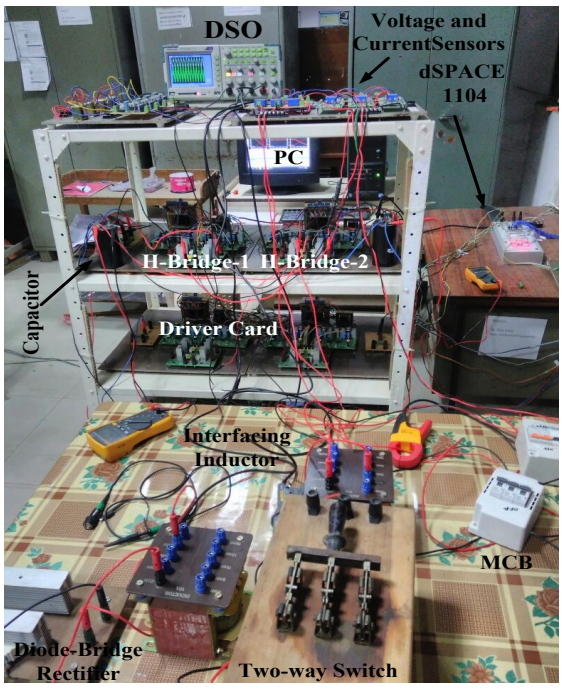


Fig. 18. SAPF performance with R-C type of loading (a) V_S with non-linear I_S (b) THD of I_S before compensation (c) V_S, I_S, I_L, I_C steady-state waveform (d) THD of I_S after compensation (e) SAPF operation with five-level voltage waveform

Appendix: Experimental Set-Up



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