Simulation and Performance Comparison of Si and SiC Based on a Proposed H6 Inverter for PV Grid-tied Applications

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Abstract- Multilevel transformerless inverters are widely employed in PV grid-tied applications because of their significant benefits in reducing switching losses and enhancing system efficiency. Wide bandgap (WBG) semiconductor devices such as SiC MOSFETs can increase the system performance and reduce the total losses due to their superior features over Si switching devices. This paper investigates a three level transformerless inverter based on H6 topology. The proposed topology is implemented with SiC MOSFETs and a modulation approach is adopted to reduce the number of conducting switches. Also, a detailed comparison of the use of SiC and Si switching devices in terms of switching and conduction losses, high switching frequency operation, filter size reduction, and thermal analysis and heat sink volume is presented. Simulation results show that total conduction and switching losses are reduced by about 50%, which allow a significant increase in either the switching frequency or the inverter power rating level for the same switching device losses. Additionally, operating at higher switching frequencies using SiC MOSFET leads to a significant reduction in volume and weight of the inductor filter. Furthermore, a thermal analysis is performed using COMSOL software to investigate the heat sink requirement.

Keywords Wide Bandgap (WBG); SiC MOSFET; photovoltaic (PV); transformerless inverter; leakage current; common mode voltage.

1. Introduction

The expected total global renewable energy generation by the end of this year is 2,017 GW [1]. One of the major renewable energy sources is photovoltaic (PV), which contributes to about 47% of the recently installed renewable power generation [1]. PV systems have been broadly installed in domestic grid-connected such as low power residential sites [2-4]. Single and three-phase PV inverters are generally used in residential areas. These inverters can be implemented with or without line transformers. Using inverter without transformer (transformerless inverter) has the advantages of high power density, high efficiency, and lower cost because of the absence of galvanic isolation. Therefore, for low power and low-cost PV application used in the residential sector, transformerless inverters become the best option due to their benefits. On the other hand, there are some drawbacks because of the absence of a transformer in transformerless inverters. One of the major issues of the absence of a line transformer is the presence of a common mode (CM) leakage current that flows through the parasitic capacitances between the PV panel and the ground [5-10]. The circulating of leakage current in the system leads to serious safety and radiated interference problems [11]. Accordingly, the value of the leakage current must be minimized and restricted to an acceptable range [12].

The leakage current path in a transformerless inverter is shown in Fig.1. The leakage current passes through a loop composed of an inductor filter (L1 and L2), ground impedance (Zg), and parasitic capacitances (CPV1 and CPV2). The equivalent circuit of the loop is describing as LC resonant

circuit that is in series with the common mode voltage [12]. The common mode voltage of the system is given by

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} + (v_{AN} - v_{BN})\frac{L_2 - L_1}{2(L_1 + L_2)} \quad (1)$$

The leakage current must be eliminated or to be minimized to a small value that does not affect the system. Therefore, to achieve a small value of leakage current, the common mode voltage must have a constant value or to be varied at a low switching frequency of 50Hz or 60Hz. The traditional solution to achieve this goal is to use a half bridge inverter [13-14].

In this type of structure, the inductor filter L2 is zero and the common mode voltage equation is simplified as

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} - \frac{(v_{AN} - v_{BN})}{2} = v_{BN} \quad (2)$$

It is observed that the common mode voltage is constant because of the direct connection between the neutral line of the grid to the centre of the split DC link capacitor. On the other hand, a half-bridge inverter utilizes half the DC voltage compared to the full-bridge inverter. Therefore, high input DC voltage is required, which can be achieved by using a large number of PV panels connected in series or by using high gain DC-DC converter placed between the PV panels and the inverter. As a result, using half-bridge inverter leads to an increase of the system cost and a degrade in the system efficiency. There are many methods and solutions proposed to achieve constant common mode voltage in transformerless full-bridge inverters [15-24]. Because the inductor filter L1 and L2 have the same value, the common mode voltage equation can be simplified as

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} \quad (1)$$

An alternative method of maintaining constant common mode voltage in the full-bridge inverter is to disconnect the AC and DC sides during the freewheeling modes. Many topologies have been derived and developed based on this method, such as highly efficient and reliable inverter concept (HERIC) [15], the H5 inverter [16], and the H6 topology [17].

In this paper, a novel H6 topology is proposed to solve the issue of the leakage current and to reduce the total power losses [25]. In this proposed topology, the number of conducting switches are reduced to five switches instead of six switches as in H5 and conventional H6 transformerless inverters. Therefore, the total conduction losses of the inverter are reduced and the efficiency of the system is improved. Additionally, the benefits of using WBG power devices, such as SiC MOSFET are discussed in detail. WBG power devices can operate at high switching frequencies and have low switching and conduction losses due to their material properties [26-27]. Therefore, a high system efficiency and high-power density can be achieved with WBG power devices such as SiC MOSFET and GaN HEMT [28-32]. There is a research gap in the literature regarding comprehensive thermal model design and heat sink requirement. Therefore, to bridge the gap, a comprehensive thermal model design is performed using COMSOL software to compare the heatsink requirement of both selected switching devices SiC MOSFET and Si IGBT.

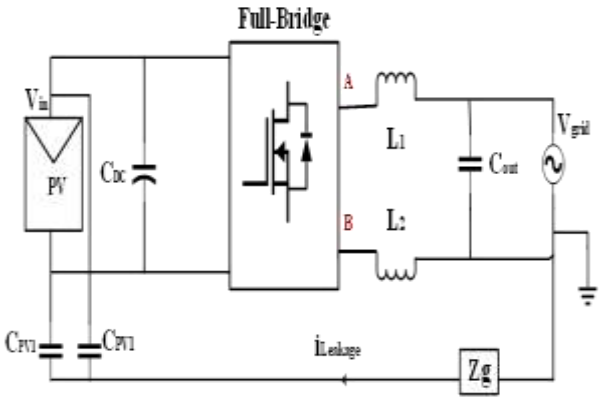


Fig. 1. Leakage current path in transformerless inverter.

This paper is organized as follows: the H6 topology and its operation modes are given in section 2. The power loss analysis is presented in section 3. The loss evaluation of SiC MOSFET and Si IGBT are investigated in section 4. Simulation results and discussion are given in section 5. Thermal model simulation and heat sink design is described in section 6. Section 7 concludes the paper.

2. Structure of the H6 Topology and its Operation Modes

2.1. Proposed H6 Topology

The schematic diagram of the proposed topology is presented in Fig 2. The proposed H6 topology is a modified version of the conventional H6 topology. In the positive half cycle, there are two switches conducting instead of three conducting switches in the conventional H6 topology. Therefore, the total conducting switches are reduced from six switches to five switches, which will result in reducing the total conduction losses.

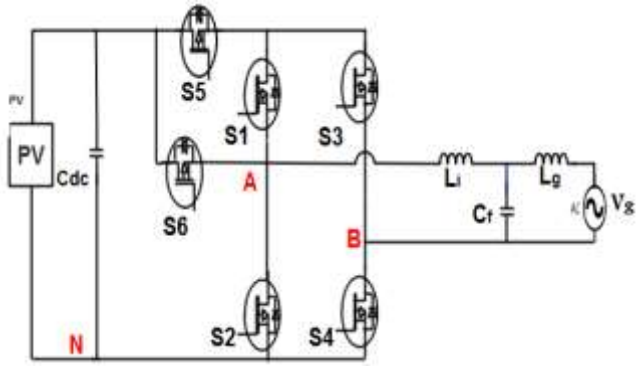


Fig. 2. Circuit structure of the proposed topology.

2.2. Proposed Operation Modes of the Proposed Topology

There are four possible operating modes. The driving signals of the proposed topology is illustrated in Fig 3.

Mode I is the active mode in the positive half period. In this mode, S1, S6 and S4 are turned ON, and the other switches are turned OFF as shown in Fig. 4(a). The inductor current is flowing through S4 and S6. Even though S3 is

turned ON, there is no current flowing through it, which means that the switch S1 has no conduction loss in this mode. The common mode voltage in Mode I is calculated as follows:

$$v_{AN} = U_{PV} \quad (4)$$

$$v_{BN} = 0 \quad (5)$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5U_{PV} \quad (6)$$

Mode II is the freewheeling mode in the positive half period. In this mode, S1 is turned ON and the other switches are turned OFF as shown in Fig. 4(b). The inductor current is flowing through S1 and the antiparallel diode of S3. The common mode voltage in Mode II is given as

$$v_{AN} = v_{BN} = 0.5U_{PV} \quad (7)$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5U_{PV} \quad (8)$$

Mode III is the active mode in the negative half period. In this mode, S5, S3, and S2 are turned ON and the other switches are turned OFF as shown in Fig. 4(c). The inductor current is flowing through S2, S3 and S5. The common mode voltage in Mode III is expressed as:

$$v_{AN} = 0 \quad (9)$$

$$v_{BN} = U_{PV} \quad (10)$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5U_{PV} \quad (11)$$

Mode IV is the freewheeling mode in the negative half period. In this mode, S3 is turned ON and the other switches are turned OFF as shown in Fig. 4(d). The inductor current is flowing through S3 and the antiparallel diode of S1. The common mode voltage in Mode IV is calculated as follows:

$$v_{AN} = v_{BN} = 0.5U_{PV} \quad (12)$$

$$v_{CM} = \frac{v_{AN} + v_{BN}}{2} = 0.5U_{PV} \quad (13)$$

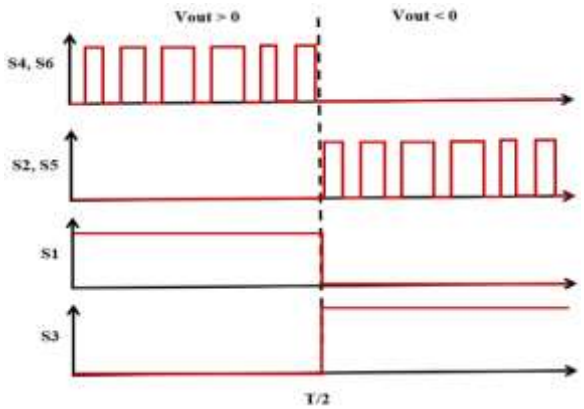


Fig. 3. PWM strategy of the proposed topology.

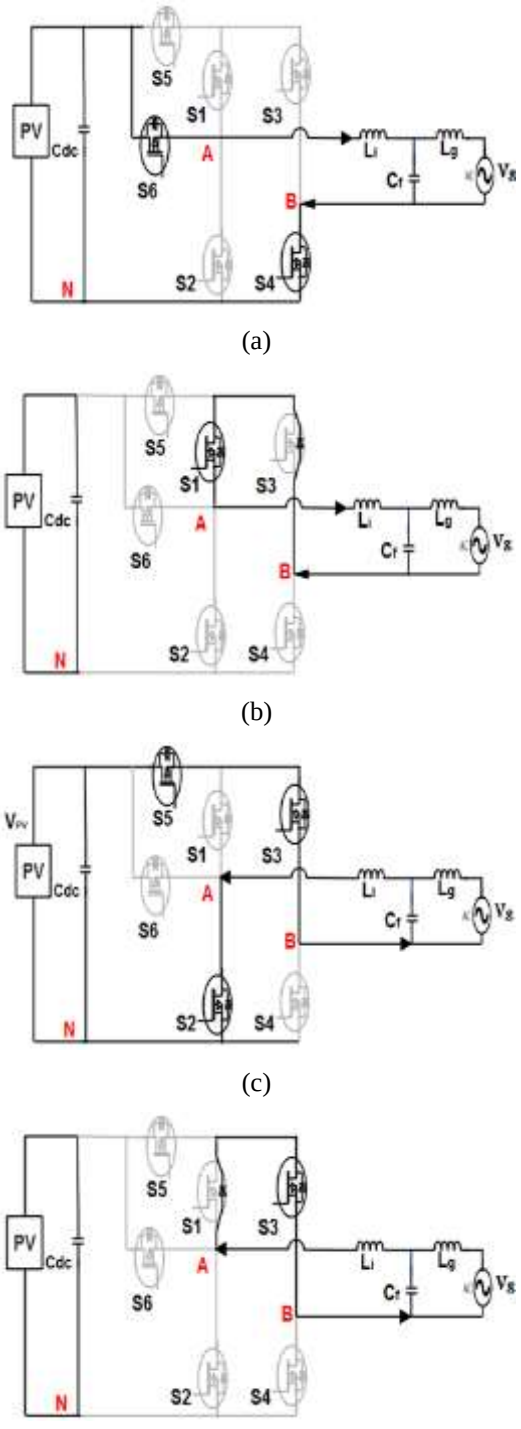


Fig. 4. Operation modes of the proposed topology. (a) The positive active state. (b) The zero state during the positive half period. (c) The negative active state. (d) The zero state during the negative half period.

3. Theoretical Switching and Conduction Power Losses Analysis

A theoretical model loss is derived for two power semiconductor devices, which are Si IGBT and SiC MOSFET. The parameters of the switching devices are given in Table 1.

Table 1. Switching devices parameters.

Parameter	IGBT (FGH15T120SMD)	SiC (C2M0080120D)
Breakdown Voltage (V)	1200	1200
Continuous Current (A)	30	36
$R_{DS\text{-}ON}/R_{CE}$ (mΩ)	28	80
V_t (V)	0.75	-
V_f (V)	0.8	1.4
R_{AK} (mΩ)	183	80
I_{RRM} (A)	7.4	10
Q_{rr} (reverse recovery charge) (nC)	270	192
T_{rr} (reverse recovery time) (ns)	183	32

To evaluate the performance of PV transformerless inverters, it is important to measure the losses of the switching devices at different output loads. The losses in semiconductor power devices can be divided into two parts switching losses and conduction losses. A detailed power loss analysis of the semiconductor power devices and diode are given in [33]. To calculate the conduction losses, first the voltage drop across these devices must be identified and is given as follows:

$$v_{DS}(MOSFET) = i(t) * R_{DS} \quad (14)$$

$$v_{CE}(IGBT) = V_t + i(t) * R_{CE} \quad (15)$$

$$v_{AK}(Diode) = V_f + i(t) * R_{AK} \quad (16)$$

Where vDS represents a drain to a source voltage drop of the MOSFET, RDS is the ON state resistance of the MOSFET, vCE is the voltage between collector and emitter in IGBT, vt indicates the corresponding voltage drop under zero-current condition, RCE stands for the IGBT ON resistance, vAK represents the voltage between the anode and cathode of the diode, Vf denotes to the diode corresponding voltage drop under zero-current condition, RAK is the ON resistance of the diode, and i(t) indicates the current passing through the device. The conduction losses can be calculated by the given equation:

$$P_{Con-act} = \frac{1}{2\pi}\int_0^{\pi} v_{cond} * i(t) * D_{act}(t) d(\omega t) \quad (17)$$

$$i(t) = I_m \sin(\omega t + \theta) \quad (18)$$

$$D_{act}(t) = M sin(\omega t) \quad (19)$$

Where Im stands for the output current peak of the inverter, w represents the angular frequency, θ denotes to the phase displacement between voltage and grid current, Dact represents the duty ratio during active state and M can take a value between 0 and 1. The conduction loss of a single switching device in the zero state is expressed as

$$P_{cond-zero} = \frac{1}{2\pi}\int_0^{\pi} v_{con} * i(t) D_{zero}(t) d(\omega t) \quad (20)$$

$$D_{zero}(t) = 1 - M sin(\omega t) \quad (21)$$

Where Dzero represents the duty ratio during zero state. The second part of the power loss is the switching loss during turn-ON and turn-OFF time. The switching ON and OFF power losses are given as

$$P_{ON} = \left(\frac{I_m \cdot V_{DC}}{2\pi}\right) \cdot f_{sw} \cdot \frac{E_{on}}{V_{test} \cdot I_{test}} \quad (22)$$

$$P_{OFF} = \left(\frac{I_m \cdot V_{DC}}{2\pi}\right) \cdot f_{sw} \cdot \frac{E_{off}}{V_{test} \cdot I_{test}} \quad (23)$$

Where Eon and Eoff are the turn-ON and turn-OFF energy losses. These energy losses are measured under accurate test conditions over different junction temperatures and reported in data sheets for given values of switching current and voltage.

The switching-ON loss of a diode can be ignored because it is too small. The diode switching-OFF loss is calculated as follows:

$$P_{Diode-OFF} = \frac{1}{12} \cdot t_b \cdot I_{RRM} \cdot \frac{V_{DC}}{2} \cdot f_{sw} \quad (24)$$

Where IRRM denotes to the reverse recovery current.

3.1. Proposed Analysis of Power Losses in the Proposed Topology

The schematic diagram of the proposed topology is presented in Fig 2. The proposed H6 topology is a modified version of the conventional H6 topology. In the positive half cycle, there are two switches conducting instead of three conducting switches in the conventional H6 topology. Therefore, the total conducting switches are reduced from six switches to five switches, which will result in reducing the total conduction losses.

The total number of conducting switches in the proposed topology is reduced to five. Therefore, total conduction losses during the active state are calculated as follows:

$$P_{co-act} = 5 \cdot (P_{con-act}(IGBT/MOS)) \quad (25)$$

There are two switching devices and two body diodes conducting in the zero state. Accordingly, the total conduction losses during the zero state are given as

$$P_{con-z} = 2 \cdot (P_{con-z}(Diode) + P_{con-z}(IGBT/MOS)) \quad (26)$$

There are four switching devices operating at switching frequency and the total switching losses are expressed as

$$P_{sw} = 4 \cdot (P_{ON} + P_{OFF}) \quad (27)$$

The range of DC link voltage of a PV system for residential applications is up to 1000 V. Therefore, switching power devices of a 1200 V rate are required for the inverter design. The most common switching power devices used for the range of 1000 V DC link are IGBTs due to their low ON-state voltage compared to Si MOSFET. On the other hand, IGBTs power devices have bipolar output characteristics that degrade their switching capability. The new development of switching power devices such as SiC MOSFETs provide an alternative and attractive solution for residential PV

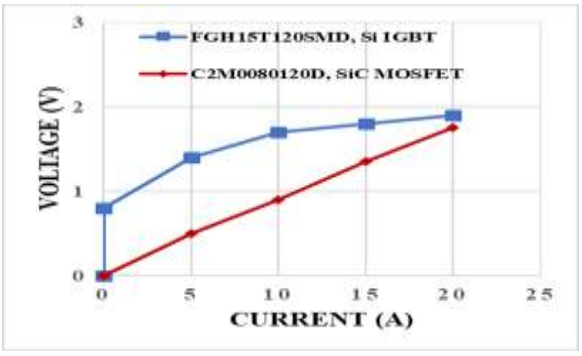
applications. SiC based devices have superior performance compared to IGBTs in the range of 1200 V due to their low ON-state resistance, small switching and conduction losses, and high switching operation frequency.

4. Loss Evaluation of Si IGBT and SiC MOSFET Power Devices

The total power loss of a switching device can be classified into two parts: switching and conduction losses. An accurate evaluation of conduction losses requires specific performance data given in datasheet, such as the ON-state resistance of MOSFET, saturation voltages of IGBT, and forward voltage of body diode [34-35]. Different parameters must be determined for the evaluation of switching energy losses such as gate drive voltage, gate resistance, and junction temperature. A double pulse test circuit is designed using LTSpice for both switching devices to get an accurate comparison of switching energy losses.

4.1. Evaluation of Conduction Losses

Conduction losses can be determined by multiplying the voltage drop across the switch when it is ON with the current flowing through the switch. Conduction losses represent a major part to the total overall semiconductor losses. The stated forward voltages of the selected switching power devices over different current values are given in Fig. 5. It is observed that SiC MOSFET has small voltage drop compared to Si IGBT because of the resistive output characteristics of the SiC MOSFET, which leads to small conduction losses.



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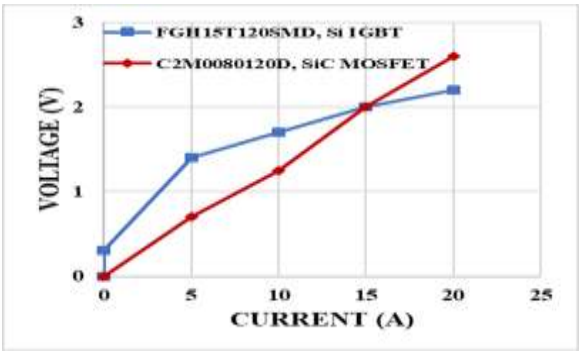
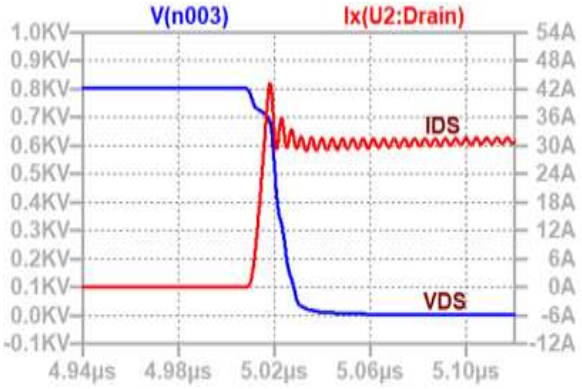


(b)

Fig. 5. Forward voltages. (a) Forward voltages of SiC MOSFET and Si IGBT at 25 ℃. (b) Forward voltages of SiC MOSFET and Si IGBT at 175 ℃.

4.2. Evaluation of Switching Losses

LTspice software is used to study the switching waveforms characteristics of the selected switching power devices. The spice models are provided by their manufacturing companies. The turn-ON and turn-OFF switching waveforms at 800 V and 30 A for the SiC MOSFET and Si IGBT are shown in Fig. 6. It is obvious that SiC MOSFET has better switching characteristics in terms of dv/dt and di/dt. At the turn off transition, the dv/dt is measured for both switching devices. It is found that SiC MOSFET switches at 19.8 kV/ms while the Si IGBT switches at 3.9 kV/ms. Table 3 presents the turn-ON and turn-OFF transition states for both switching devices.



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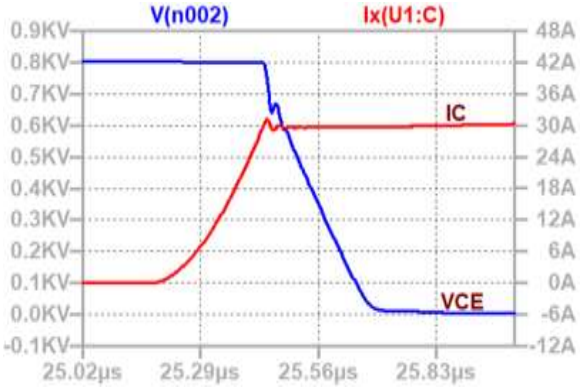

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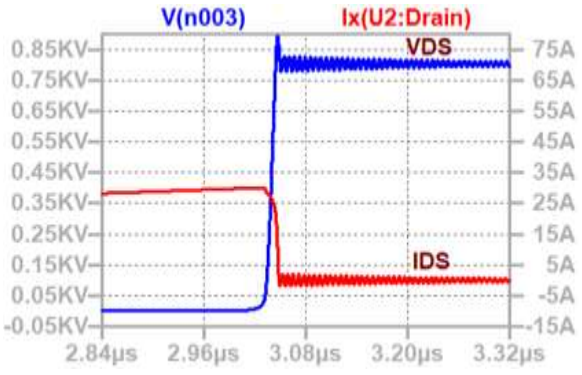

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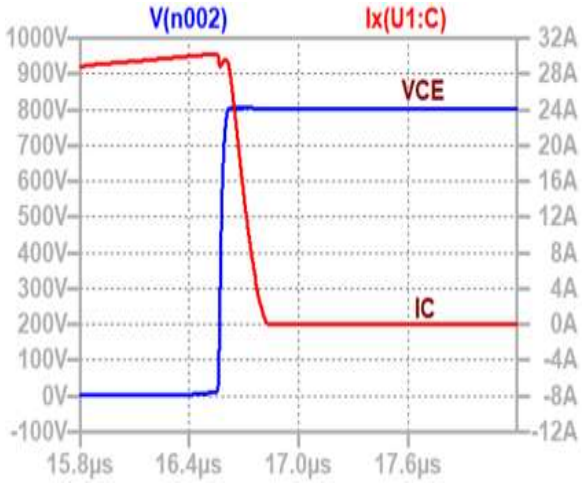


(d)

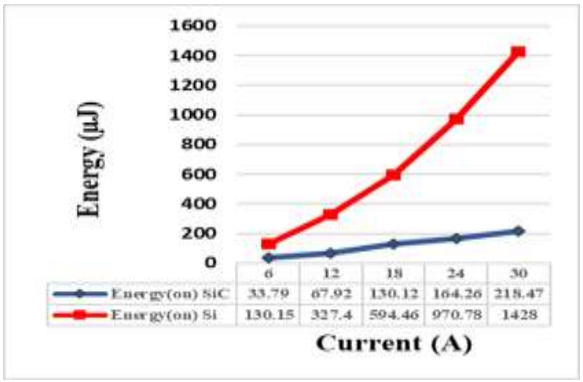
Fig. 6. Switching transitions of switching devices for a voltage of 800 V and 30 A. (a) Turn-on SiC MOSFET. (b) Turn-on Si IGBT. (c) Turn-off SiC MOSFET. (d) Turn-off Si IGBT.

Table 2. Turn-On and turn-Off switching transition.

	Turn-on		Turn-off	
	Si IGBT	SiC MOSFET	Si IGBT	SiC MOSFET
$\frac{dv}{dt}\left(\frac{kV}{\mu s}\right)$	5	23	3.9	19.8
$\frac{di}{dt}\left(\frac{kA}{\mu s}\right)$	0.35	1.4	0.12	2

The switching energies can be calculated by integrating the area resulted from the product of the voltage and current. By applying this method, the measured turn on and turn off energies of both switching devices are given in Fig. 7.

The turn-ON switching energy losses are small compared to the turn-OFF switching energy losses for both switching devices. The study shows that at low current levels, the Si IGBT must dissipate more than 3 times the turn on energy of the SiC MOSFET. Therefore, the switching energy losses of Si IGBT is much larger and it increases linearly with current. However, SiC MOSFET has very low turn-OFF energy losses, which can be a major advantage compared to Si IGBT. Also, the total energy loss of SiC MOSFET has increased slightly when the temperature is increased to 100℃. The turn-OFF energy losses of the Si IGBT are about 8 times higher than SiC MOSFET at a current of 6 A and about 10 times higher at a current of 30 A as shown in Fig. 7(b). The drawback of Si IGBT is that it has large switching energy losses. As a result, SiC MOSFET is an attractive solution for high switching frequency application because of its superior switching characteristics.



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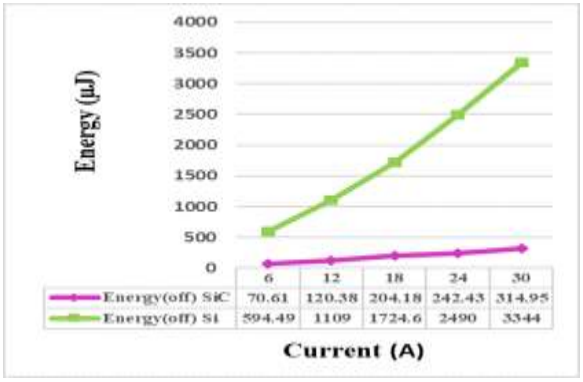

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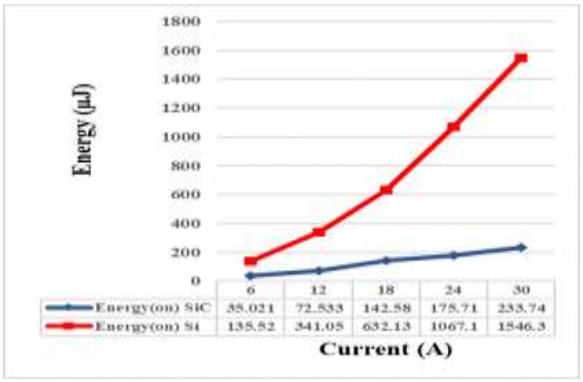

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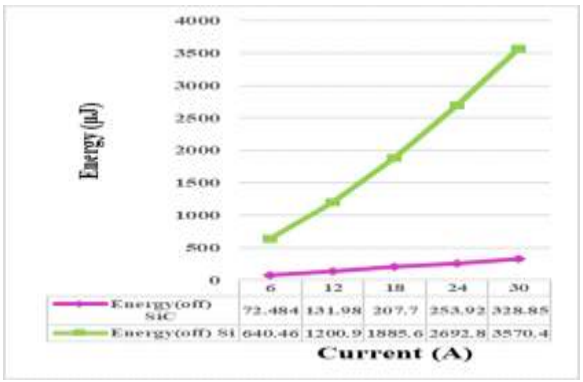


(d)

Fig.7. Turn-on and turn-off switching energy losses for a voltage of 800 V and 30 A. (a) Turn-on energies at 25℃ . (b) Turn-off energies at 25℃. (c) Turn-on energies at 100℃. (d) Turn-off energies at 100℃.

5. Simulation Results and Discussion

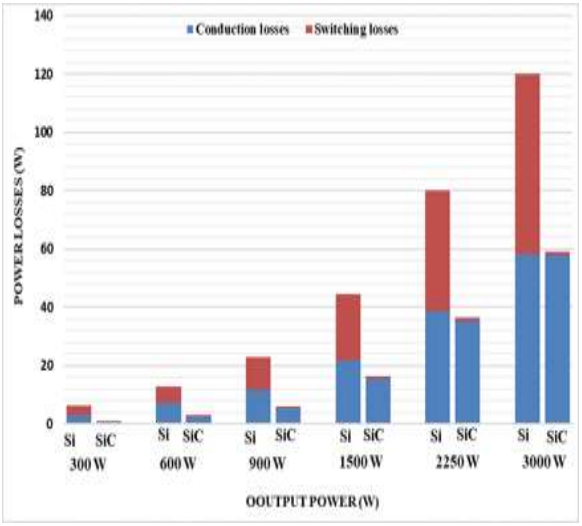
The proposed inverter is designed and simulated using PSIM simulation software. The specifications of the system design are given in Table 2. The benefits of implementing SiC MOSFET instead of Si IGBT is studied and demonstrated in this section.

Table 3. Specifications of the system design.

Parameter	Value
Input Voltage	800 V
Grid Voltage	120 V
Grid Frequency	60 Hz
Switching Frequency	16 kHz and 100 kHz
DC bus capacitor (C_{DC})	970 µF
Output Power	2 kW

5.1. Efficiency Improvement

Semiconductor losses have a significant impact on the inverter efficiency. The semiconductor losses for Si IGBT and SiC MOSFET over different output power loads at 16 kHz are presented in Fig. 8. It is observed that SiC MOSFET has low conduction losses at light loads because it has resistive output characteristics. Moreover, at a full output power load of 3 kW, the conduction losses of the Si IGBT are almost the same as in SiC MOSFET because Si IGBT has a constant voltage drop. On the other hand, the major benefit of using SiC MOSFET is its low switching losses due to the absence of tail current. The total losses are reduced by more than 50% with SiC MOSFET as shown in Fig. 8(a). The semiconductor losses with different output power loads at 100 kHz are given in Fig 8(b). The total power loss of the Si IGBT at 100 kHz is about four times higher than that at 16 kHz, which means that Si IGBT is not suitable for high switching frequency applications. On the other hand, the total power loss of SiC MOSFET is increased by only 12% at 100 kHz.



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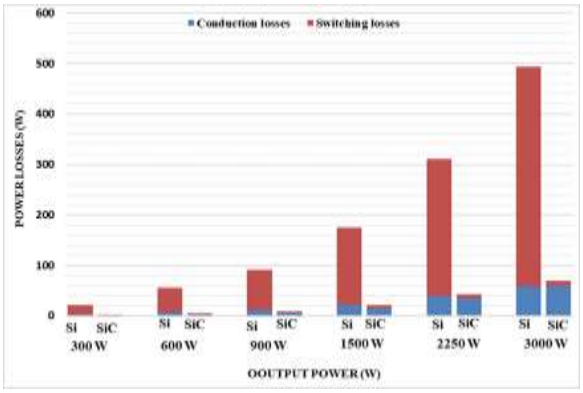


(b)

Fig. 8. Conduction and switching losses of Si IGBT and SiC MOSFET with different output power loads: (a) at 16 kHz. (b) at 100 kHz.

The efficiency of the system with different output power loads at two different switching frequencies is illustrated in Fig. 9. The efficiency of the system at 16 kHz is increased by 2% with SiC MOSFET. The benefits of using SiC MOSFET become more obvious at higher switching frequencies where the efficiency of the system increased by almost 14% compared to Si IGBT at 100 kHz.

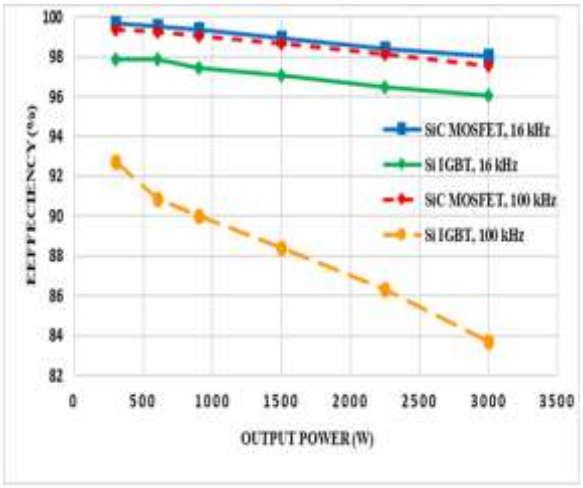


Fig. 9. Efficiency comparison between Si IGBT and SiC MOSFET with different output power loads and at two different switching frequencies.

5.2. Switching Frequency versus Inductor Volume

Semiconductor The simulation results verified that SiC MOSFET can operate at high switching frequency while maintaining low power losses. The value of the inductor is inversely proportional to the switching frequency and it is given by the following equation

$$L = \frac{V_{DC}}{4 \cdot f_{sw} \cdot i_{max} \cdot \Delta i_{ripple}} \tag{28}$$

Where VDC is the DC bus voltage, fsw denotes to the switching frequency, imax is the peak current, and Δripple is the current ripple and choose to be 20% of the peak current.

A significant reduction in the inductor volume can be

achieved when the switching frequency increases to higher values. In this study, the switching frequency of the system increased to 300 kHz with SiC MOSFET until the power losses become the same as in Si IGBT at 16 kHz as shown in Fig. 10.

The inductor value at different switching frequencies is presented in Fig. 11. The inductor value is decreased from 1400 µH at 20 kHz to 140 µH at 200 kHz. The large reduction in the inductor value leads to small size and volume of inductor storage.

The core material used in this study for the sake of comparison is a toroid core manufactured using Kool Mu material. The effect of increasing the switching frequency on the magnetic core volume is presented in Fig. 12. This study shows that as the switching frequency increases the magnetic core volume decreases. The magnetic core volume decreased from 220 cm3 at 20 kHz to 20.7 cm3 at 200 kHz. Moreover, a smaller inductor volume leads to a smaller inductor weight. The relationship between the switching frequency and the inductor weight is shown in Fig 13. The inductor weight is reduced from 1200 g at 20 kHz to 120 g at 200 kHz.

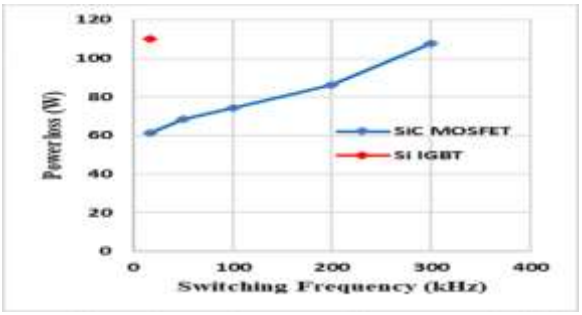


Fig. 10. Switching frequency versus power losses for SiC MOSFET and Si IGBT.

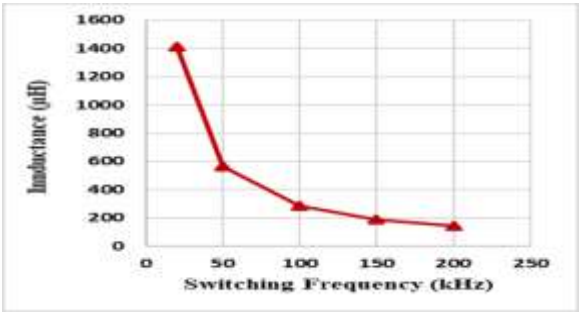


Fig. 11. Switching frequency versus inductor values.

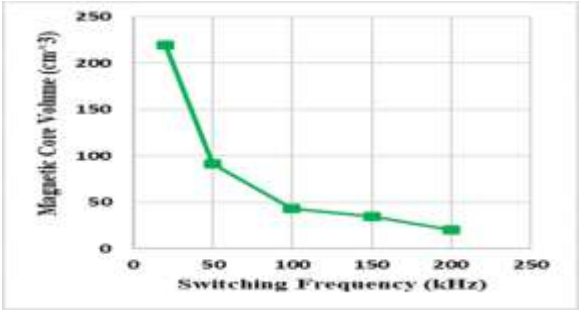


Fig. 12. Switching frequency versus magnetic core volume.

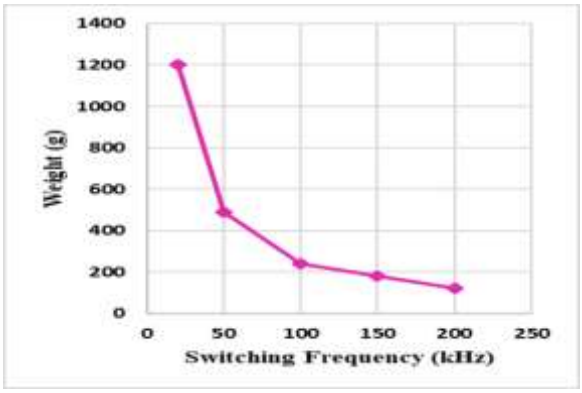


Fig. 13. Switching frequency versus inductor weight.

5.3. Switching Power Rating Increasing

As explained previously, using SiC MOSFET instead of Si IGBT leads to a significant reduction in the total power losses. Therefore, the power rating of the inverter could be increased by adding more power to the load without modifying the size of the heatsink. The output of the inverter can be increased from 1.7 kW using Si IGBT to 3 kW using SiC MOSFET for the same total power semiconductor losses as illustrated in Fig. 14. In other words, the power rating of the system can be increased by more than 75% with SiC MOSFET.

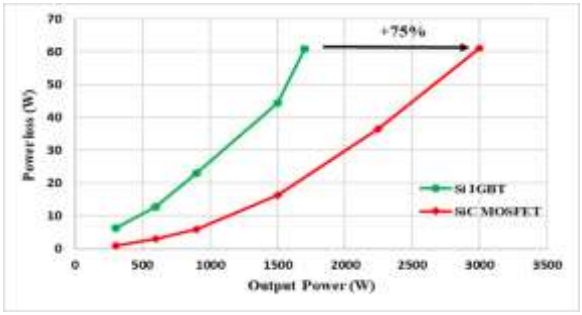


Fig. 14. Increased power rating with SiC MOSFET for the same power semiconductor losses.

5.4. Thermal Model Simulation and Heat Sink Design

The use of simulation software for modelling thermal performance of heatsinks is not new and has been reported in literature [36-40]. Commercial software like COMSOL Multiphysics, FLUENT, ANSYS, Pro-MECHANICA etc. are prime examples of simulation software that use numerical methods, Finite Element and Finite Volume Methods (FEM and FEV) along with Computer Aided Design (CAD) tools to model the thermal performance of heatsinks.

For the purposes of this paper, COMSOL Multiphysics was used to create two identical 3D models of a 6-pack MOSFET module with Silicon (Si) and Silicon Carbide (SiC) as their respective semiconductor materials. Heatsinks were added to these MOSFET modules to reduce the structures' temperatures and to compare each semiconductor's thermal performance. COMSOL solved for the temperatures of the 3D structure using Finite Element Analysis (FEA). Boyd Corp's online tool AAVID Genie was used to verify the results of the

simulated structures with their commercially available heatsinks that were simulated in COMSOL. The Heat Transfer in Solids module of COMSOL simulated the thermal aspects of the models. The Joule heating generated by electric currents passing through each of the MOSFET modules were obtained from calculations made in PowerSim which acted as the heat sources for COMSOL. A stationary study was created for each model to study the steady state effects of the Joule heating on the temperature of each structure. The physical dimensions of both MOSFET modules were kept the same and were obtained from the CREE 1200V, 50A 3-Ph SiC MOSFET module [32]. The dimensions of the heatsink for the SiC model were made smaller to demonstrate the superiority of the Wide Bandgap (WBG) material SiC in terms of heatsink requirements for similar steady state temperatures. Thermal stresses and physical deformation were not simulated for the purposes of this paper.

5.4.1 Model Geometry

The internal structure the CREE 1200V, 50A 3-Ph SiC MOSFET module consists multiple layers and components. The dimensions of this internal structure were obtained from [33] to create the 3D CAD model of the module in COMSOL. The module starts from the bottom to the top with a Copper (Cu) Baseplate, a solder layer, a Copper layer, an Aluminum Nitride (AlN) layer and a Copper layer [41]. Six sets of MOSFETs and Diodes are soldered on top of the final Copper layer [41]. The dimensioned 3D view, the yz-plane view and the xy-plane view of the MOSFET modules are shown in Fig. 15, Fig. 16 and Fig. 17 respectively. Figure 16 is scaled to make all the layers viewable. The MOSFETs and diodes were set to be of the same semiconductor material i.e. Si and SiC for their respective models.

Fig. 15. 3D view of MOSFET module.

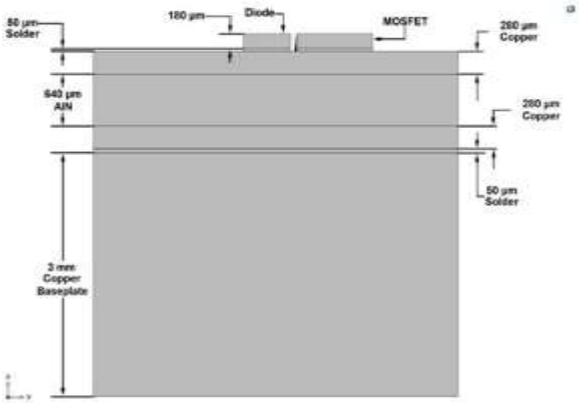


Fig. 16. YZ-plane view of the module.

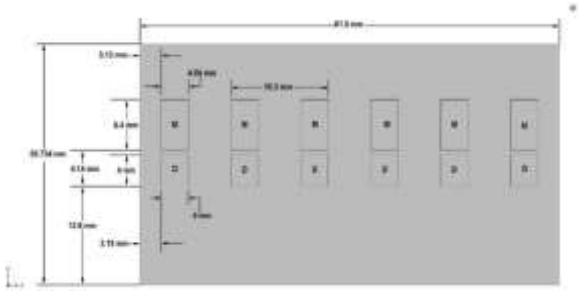
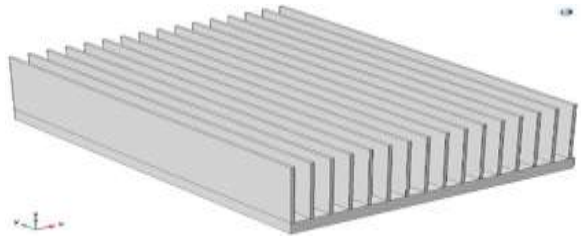
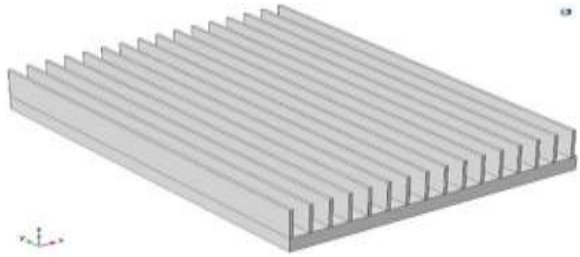


Fig. 17. Xy-plane view of the module.

The final layer of each model consisted of an Aluminum (Al) heatsink which rested on top of the MOSFET and diode layers. The dimensions of the heatsinks were obtained from Boyd Corp's online tool AAVID. These dimensions were based on real world heatsinks sold by Boyd Corp that would make the maximum temperatures of the module-heatsink combinations below 100 ºC. The heatsinks used for the Si and SiC modules are shown in Fig. 18(a) and (b) respectively. Each heatsink consists of a solid Aluminum block of dimensions 141.8 mm× 104.3 mm.× 6.6 mm. A total number of 16 aluminum fins of width 1.134 mm and separated by 6.8 mm were added on top of this block with heights of 33.5 mm and 13.4 mm for the Si and SiC models respectively.



(a)



(b)

Fig. 18. Heatsink structure for: (a) Si model. (b) SiC model.

5.4.2 Material Properties

The physical material properties used for the models were the Density ρ, the Heat capacity at constant pressure (Cp) and Thermal conductivity (k). Only these three properties were used for the simulations because heat transfer in solids was the only physics being studied. The materials were assumed to be isotropic with every property considered to be constant in all 3 directions. The properties for all materials simulated in the models except for the Solder were obtained from built-in libraries in COMSOL. SAC396 solder, an alloy of Tin, Silver and Copper, was chosen for the models and its properties were obtained from [42]. The material properties for all the materials used are given in Table 4.

Table. 4 Thermal properties of materials used. .

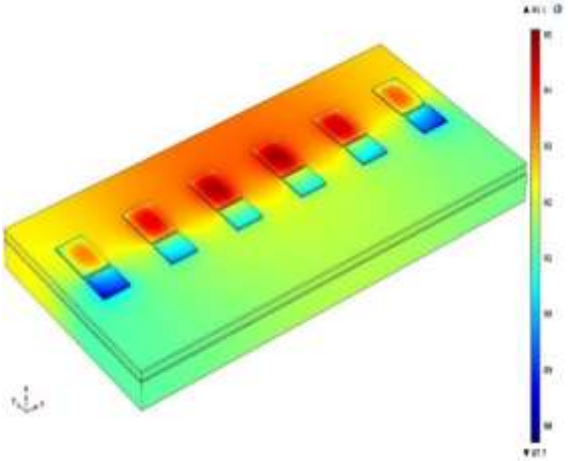
Property	Symbol	Unit	Cu	SA C396	AIN	Si	SiC	Al
Density	ρ	kg/m^3	8960	7400	3260	2329	3216	2700
Heat capacity at constant pressure	C_p	J/(kg.K)	385	220	740	700	690	900
Thermal conductivity	k	W/(m.K)	400	61.1	160	131	490	238

5.4.3 Heat Transfer Physics Modeling

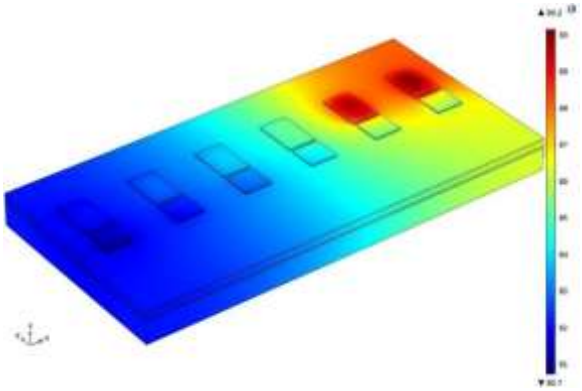
The heat transfer in solids physics module of COMSOL was used to simulate the thermal performance of each MOSFET-heatsink structure. The heat losses calculated from PowerSim for each MOSFET in each semiconductor model were input as heat sources for the simulations. For the Si model, these losses for the MOSFETs, going from left to right in Fig. 1, were 19.85 W, 19.85 W, 19.85 W, 19.85 W, 20.4 W and 20.4 W while for the SiC, the losses were 4.1 W, 4.1 W, 4.1 W, 4.1 W, 22.25 W and 22.25 W respectively. As the heatsinks dissipate thermal energy from the heat generated by the MOSFETs to the surrounding air, a convective heat flux boundary condition for all heatsink surfaces in contact with air was set up. The convective heat transfer coefficient was given a value of 10.45 W/m^2.K to simulate non-forced free flowing air. The initial temperature of the structures and surrounding air was set to room temperature i.e. 293.15 K or 20 ºC. Using these inputs and boundary conditions, COMSOL solved the heat equation in solids to obtain the temperature profiles of each model.

5.4.4 Model Simulation and Results

The temperature profile of the Si and SiC models with the heatsinks hidden are shown in Fig. 19 and 20. The temperature profiles for the Si and SiC models with the heatsinks visible are given in Figures 21 and 22. The temperatures displayed on the legends are in ºC.



(a)



(b)

Fig. 20. Temperature profile of SiC model with heatsink not visible.

The temperature profiles for the Si and SiC models with the heatsink not visible show that the highest of temperatures are concentrated around the MOSFETs that have the highest heat losses. As the heat losses for all Si IGBTs are close to 20 W, the temperatures are fairly uniform throughout the Si MOSFET module structure whereas for the SiC model, the temperatures are higher at the right end near the MOSFETs with losses of 20.25 W losses while the left end with lower losses has lower temperatures.

The temperature profiles for the two models with the heatsink visible also show similar distribution of temperatures. The Si model has higher temperatures on the heatsink fairly uniform around all the IGBTs while the SiC model has higher temperatures more concentrated at the right end where the MOSFETs with higher losses are located.

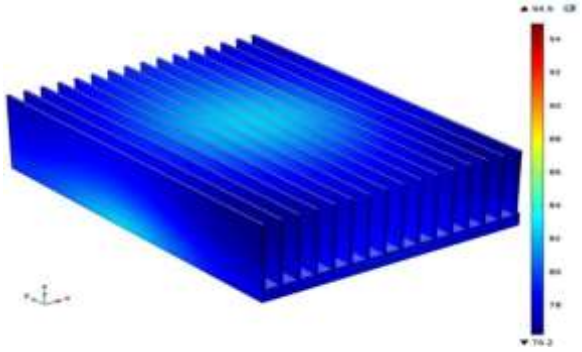


Fig. 21. Temperature profile of Si model with heatsink visible.

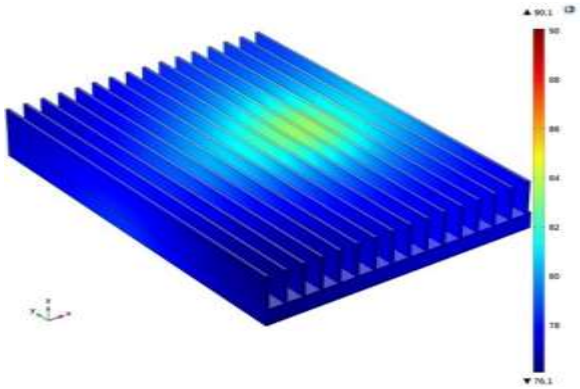


Fig. 22. Temperature profile of SiC model with heatsink visible

The maximum temperatures for the Si and SiC models were found to be 95.15 ºC and 90.18 ºC respectively. The minimum temperatures were 76.23 ºC and 76.10 ºC for the Si and SiC models respectively. The 3D model for Si IGBTs had a volume of 183.8 cm3 and surface area of 1861 cm2 for the heatsink. The SiC model had a volume of 132.1 cm3 and surface area of 941.2 cm2. From the simulations for the two models, it is clear that the SiC MOSFET module requires a smaller heatsink (by a factor of .505 in terms of surface area) for similar maximum temperatures. High temperatures are more uniform in the Si model while only the areas with higher losses have high temperature concentrated areas throughout the overall volume of the MOSFET module with SiC. The thermal modelling clearly demonstrates that the SiC module is more efficient in terms of heatsink size and overall heat dissipation.

6. Conclusion

This In this paper, a proposed H6 topology is investigated. The proposed topology succeeds in achieving constant common mode voltage and reducing the total conduction losses because there is a total of five conducting switches instead of six switches in the conventional H6 topology. The main goal of this paper is to explore and compare in detail the benefits of using SiC MOSFET instead of Si IGBT in terms of switching and conduction losses, higher switching frequencies, and thermal analysis and heatsink requirement. The total switching and conduction losses are reduced by 50% at 16 kHz with SiC MOSFET and the efficiency increased from 96% to 98%. The benefits of using SiC devices become more obvious at high switching frequency of 100 kHz where the efficiency increases by about 14%. The significant reduction of the total switching and conduction losses opens the possibilities of increasing the inverter power rating level with SiC MOSFET. For example, the power rating of the inverter at 16 kHz with Si IGBT is increased by 75% from 1.7 kW to 3 kW with the same power losses when SiC MOSFET is used. Furthermore, SiC MOSFET has superior switching characteristics, which allow the system to increase its switching frequency by a factor of 15 while still having the same power semiconductor losses for a Si IGBT based inverter. By taking advantage of this benefit, the volume and weight of the inductor filter reduced dramatically from 220 cm3 to 20.7 cm3 and from 1.2 kg to 120 g, respectively. Finally, thermal analysis shows that SiC MOSFET requires smaller heatsink compared to Si IGBT under the same switching frequency and output power load. Accordingly, SiC devices are an attractive solution for residential PV applications that require high efficiency and small converter size.

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