Modelling of a Solar Array Simulator based on Multiple DC-DC Converters

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Received: 08.08.2017 Accepted:29.11.2017

Abstract- This paper presents a solar array simulator (SAS) to emulate the actual characteristics of solar arrays under different environmental conditions and load variations. SASs are essential in the evaluation of maximum power point tracking (MPPT) algorithms and their power converters. The proposed SAS adopts a modular structure where multiple voltage-controlled buck DC-DC converters are adopted. An active current distribution control is proposed to achieve a balanced current in the parallel connected converters. The effect of the proposed controller on the circulating current impedance is analysed, and the controller's parameters are designed to obtain excellent current distribution and fast dynamic response. The SAS's performance is explored through a Simulink model with a variable resistor load and at different irradiance levels. The results confirm the validity of the proposal, in which excellent performance was obtained in terms of tracking the desired V-I characteristics and the current distribution between the converters.

Keywords Solar array simulator (SAS); PV simulator; dc-dc converter; parallel dc-dc converters; current-voltage characteristic.

1. Introduction

Due to the shortage and increasing cost of conventional energy resources, renewable energy (e.g. wind and solar) has received great interest in recent decades [1-4]. However, new resources like photovoltaic (PV) cells have extremely nonlinear characteristics [5, 6], which are influenced by the variations in the environmental conditions (e.g. temperature, irradiance). For this reason, power converters and a maximum power point tracking (MPPT) algorithm should be attached to the PV panel to extract maximum output power [7, 8]. Solar array simulators (SASs) are frequently used during testing, implementation of MPPT techniques and evaluation of power converters under different weather and load conditions. This reduces the installation time and minimises the possibility of any destructive effects on the actual PV panels. For these reasons, SASs have attracted a great deal of attention.

Solar array simulator is a power electronic converter capable of developing the output characteristics of a real solar array at different environmental conditions and load variations [9], and it should be able to operate at different power levels [10]. The simulators can be classified according to power stage type and the schemes of reference voltage-current generation. The power stages can be either a linear or switching converter (e.g. single-phase buck, three-phase ac-dc, full bridge dc-dc, and LLC resonant converter) [4]. There are three reference generation schemes in these simulators. In the first, referred to as a voltage controlled converter, the output current is sensed and a reference generator produces the desired reference voltage [3, 11]. The second category is a current controlled converter where the desired current is generated according to the output voltage [4, 12]. In the last category, both current and voltage controlled schemes are used and the voltage control is activated during the operation between the maximum power point (MPP) and the open circuit point in the V-I curve. In the opposite scenario, the current controlled scheme is activated between the MPP and the short circuit point [13] in the V-I curve.

The high cost of commercial SASs has prompted researchers to develop several custom versions. To improve the cost and implementation time, a commercial converter has been adopted and modified to comply with SAS requirements [3]. The output current is sensed and, according

to a predefined relation, an analogue variable voltage is generated. This voltage is injected into the converter feedback loop to make the converter output voltage track the desired static V-I curve. Notwithstanding the reduced cost and time, this proposal requires the calculation of the injected voltage, and the SAS dynamic behaviour is restricted by the commercial converter crossover frequency, which is beyond adjustment. A hybrid reference generator has been proposed, and the V-I curve data collected from the actual solar cell with an adjustable light source [4]. This is combined with a high power and improved efficiency three-phase ac-dc rectifier stage with a three-phase dc-dc converter to improve the transient response and reduce current and voltage ripple. However, this PV simulator is not easily extended to a higher power level and requires a high-performance processor. A current controlled push-pull forward converter employed in a PV simulator is proposed [14]. The output voltage is measured and the reference current is generated according to the desired V-I characteristic. However, a lack of emulation in the region close to the open circuit point can be observed. To overcome this limitation, a bidirectional converter has been proposed to allow stable operation around the open circuit point region [8].

All these strategies, suffering from lack of emulation in some region in the VI characteristics, adopt a power stage not easy to be controlled and extended to a higher power level and/or heavy computations are used in their control algorithm

This paper presents a modular SAS using multiple dc-dc converters to increase the power level and enhance system efficiency and reliability [15]. Furthermore, minimal voltage and current ripple can be obtained. However, uneven current distribution or circulating current between converters is a main concern when a multiphase converter or parallel-connected converters are adopted; therefore, a suitable control method should be used to tackle this issue. A droop method which emulates a series virtual resistor at the converter's output has been extensively used to enhance the current distribution between converters. Nevertheless, this control mechanism affects the converter's voltage regulation [16]. A master-slave control approach has been proposed to restrain the imbalance current distribution between converters [17]. However, low robustness is a major concern in most master-slave mechanisms as any failure in master unit suspends the operation of the whole current distribution controller [15]. A model predictive control (MPC) scheme has been proposed in which excellent current balancing was achieved in a multi-phase buck converter [18], although the MPC algorithm requires a high-performance processor due to complex computations. A simple current distribution control scheme is proposed in this paper to attain even current distribution between the multiple dc-dc converters of the solar array simulator. This scheme is simple, modular and a high-performance processor is not necessary in its implementation. Each converter has two control loops without any communication between converters. The output voltage is controlled by an external loop, while the current sharing is adjusted with the inner current loop.

2. Proposed Method

Figure 1 shows the block diagram of the proposed simulator. Voltage controlled, parallel-connected buck dc-dc converters are employed as a power stage of the simulator, and

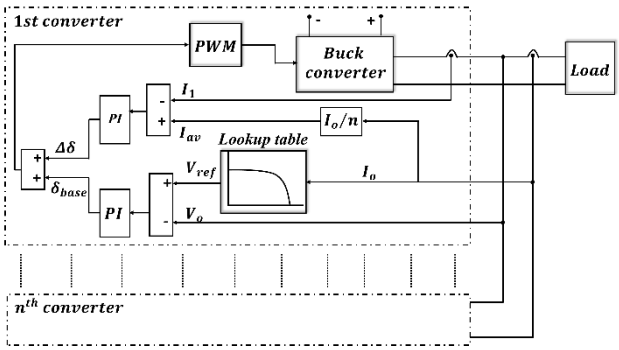

Fig. 1. Block diagram of the proposed SAS.

the continuous conduction mode is adopted in the converter operation. The total load current is measured with current sensor and feeds all parallel-connected converters.

The current value is fed to the individual converter's lookup table to generate the reference voltage. This lookup table is generated through digitising the V-I curves of the actual solar array at different irradiance and temperature levels. The reference voltage is compared with the actual voltage and the error signal fed to the PI compensator to produce the base duty cycle (δ_{base}).

The main issue with parallel-connected converters is the circulating current, which can lead to unequal current distribution and damage to the converter. To prevent this, the parallel-connected converters should have the same pulse width modulator parameters, physical parameters, and equal dead time between the two switches of the synchronous buck converter. Though this is impractical, an active control method becomes necessary to ensure even current distribution.

Improved current distribution is obtained through the emulation of virtual resistance in the circulating current path. This is achieved by adopting an average current sharing control scheme. The total load current is sensed and divided by the number of parallel units (n) to obtain the desired average current(I_o/n). The difference between the desired value and converter current is used by the PI compensator to produce the necessary duty cycle deviation $(\Delta\delta)$ to force equal current sharing between converters. In this approach, the circulating current impedance is increased and an almost even current distribution is obtained. It is clear that this proposed structure is modular and can be easily extended to any number of units, as no information is shared between the converters, except for the desired irradiance level that is supplied to the converters.

3. Mathematical Analysis

The schematic of the synchronous buck converter is shown in Fig.2 and the jth converter model with closed loop

voltage control is shown in Fig.3. The converter is modelled as a linear amplifier with gain equalling the input voltage Vg. The amplifier output is fed to an LC low pass filter to produce the output voltage. A PI compensator Gc1(s) generates the desired duty cycle to minimise the error between the reference and output voltages. The effect of dead time and the switching device voltage drop is modelled as a voltage drop in the

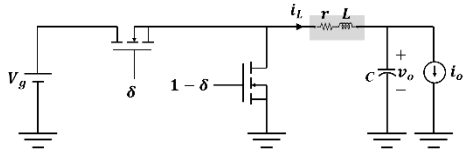

Fig. 2. Buck converter circuit diagram.

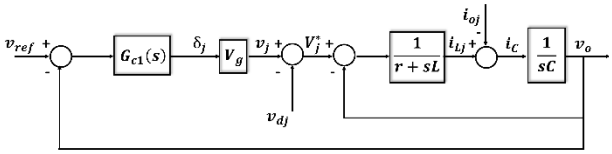

Fig. 3. Converter model with dead time and switching device voltage drop effect.

converter circuit and referred to as v_d [19]. In parallel connected, the deviation in this voltage drop v_d is a main reason for the uneven current distribution. Therefore, this effect is modelled as a disturbance voltage in the buck converter model. Applying superposition theorem on Fig. 3, the output voltage of the jth converter $(v_o(s))$ is expressed as:

$$v_o(s) = v_{refj}(s)G_1(s) - i_{oj}(s)G_2(s) - v_{dj}(s)G_3(s) \quad (1)$$

Where, $v_{ref}(s)$ is the control input voltage and $i_o(s), v_d(s)$ represent disturbance inputs. $G_1(s), G_2(s)$ and $G_3(s)$ are closed loop transfer functions defined as below.

$$G_1 = \left.\frac{v_o(s)}{v_{ref}(s)}\right|_{v_{dj},i_{oj}=0} = \frac{G_{c1}V_g}{s^2LC + srC + 1 + G_{c1}V_g};$$

$$G_2 = \left.\frac{v_o(s)}{i_o(s)}\right|_{v_{ref},v_{dj}=0} = \frac{sL + r}{s^2LC + srC + 1 + G_{c1}V_g};$$

$$G_3 = \left.\frac{v_o(s)}{v_{dj}(s)}\right|_{v_{ref},i_{oj}=0} = \frac{1}{s^2LC + srC + 1 + G_{c1}V_g};$$

$$G_{c1} = k_{p1} + k_{i1}/s$$

The inductor, inductor's internal resistor and the output capacitor for individual converters are assumed to be equal. Simplification of Eq. (1) gives the output current for the j^{th} converter as:

$$i_{oj} = 1/G_2\left[v_{refj}G_1 - v_{dj}G_3 - v_o\right] \quad (2)$$

According to Eq. (2), converters have the output current as:

$$i_{o1} = 1/G_2\left[v_{ref1}G_1 - v_{d1}G_3 - v_o\right] \quad (3-1)$$

$$i_{o2} = 1/G_2\left[v_{ref2}G_1 - v_{d2}G_3 - v_o\right] \quad (3-2)$$

……..

$$i_{oj} = 1/G_2\left[v_{refj}G_1 - v_{dj}G_3 - v_o\right] \quad (3-j)$$

……

$$i_{on} = 1/G_2\left[v_{refn}G_1 - v_{dn}G_3 - v_o\right] \quad (3-n)$$

If equally rated buck converters are assumed, the average load current (i_{av}) can be defined as:

$$i_{av} = \frac{1}{n}\sum_{j=1}^{n} i_{oj} = \frac{1}{n}i_o \quad (4)$$

Where i_o is the total load current. Substituting Eq. (3) in Eq. (4) yields:

$$i_{av} = 1/G_2\left[v_{ref\_av}G_1 - v_{d\_av}G_3 - v_o\right] \quad (5)$$

From Eq. (5) and Eq. (3), the current deviation or the circulating current can be expressed as:

$$i_{av} - i_{oj} = 1/G_2\left[\left(v_{refav} - v_{refj}\right)G_1 - \left(v_{dav} - v_{dj}\right)G_3\right] \quad (6)$$

From Eq. (6), it is evident that the current deviation or the circulating current between the converters is due to the differences in the reference voltage, dead time, and the switches' voltage drop. The impedance in the path of the first and second components of circulating current is G_2/G_1 and G_2/G_3, respectively. Unlike in dc-ac converters, the first component contribution can be easily minimised when all converters are well synchronised or a master controller is utilised to generate the reference voltage. Therefore,

$$v_{ref1} = v_{ref2} = v_{refj} = v_{ref\_av} \quad (7)$$

Accordingly, Eq. (6) is reduced to Eq. (8) as:

$$i_{av} - i_{oj} = 1/G_2\left[\left(v_{dj} - v_{dav}\right)G_3\right] \quad (8)$$

When the proposed method (Fig. 1) is activated, the buck converter with the current distribution control is modelled as in Fig. 4. The converter's current deviation from the average value $(i_{av} - i_{oj})$ is utilised by a suitable compensator $(H(s))$ to produce the desired duty cycle deviation $\Delta\delta$ to retain the equal current distribution between converters. In this case, the output voltage of the j[th] converter becomes:

$$v_o(s) = v_{ref}(s)G_1(s) - i_{oj}(s)G_2(s) - v_{dj}(s)G_3(s) + G_4\left(i_{av} - i_{oj}\right) \quad (9)$$

Where

$$G_4 = \frac{HV_g}{s^2LC + srC + 1 + G_cV_g};$$

Using Eq. (9), the output current of the j[th] converter can be expressed as:

$$i_{oj} = 1/(G_2 + G_4)\left[v_{ref}G_1 - v_{dj}G_3 + i_{av}G_4 - v_o\right] \quad (10)$$

Following the same procedure of derivation Eq. (3) to Eq. (6), yields:

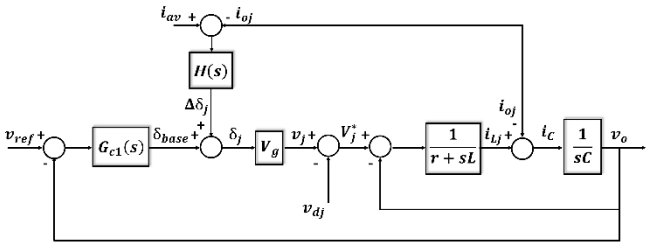

Fig. 4. Buck converter model with proposed sharing control.

$$i_{av} - i_{oj} = 1/(G_2 + G_4)\left[(v_{dj} - v_{d_{av}})G_3\right] \quad (11)$$

Compared with (8), equation (11) clearly indicates that the effective circulating current impedance is increased from (G_2/G_3) to $((G_2 + G_4)/G_3)$. The circulating current can thus be significantly reduced with suitable compensator parameters.

4. Stability Analysis

To consider the sampling and computation delays, the transfer function $D(s)$is inserted in the forward path. It can be approximated as [20]:

$$D(s) \approx \frac{1}{1 + sT_d} \quad (12)$$

To evaluate the current distribution controller, the control block diagram for the jth converter is re-arranged as in Fig. 5. The current sharing compensator $H(s)$ produces the desired deviation in duty cycle $\Delta\delta_j$ such that i_{oj} tracks i_{av}. The compensator must be designed to ensure the system stability and even current distribution between converters. Therefore, the loop transfer function $i_{oj}(s)/i_{av}(s)$ is expressed as:

$$G_T(s) = \frac{i_{oj}(s)}{i_{av}(s)} = \frac{V_g.D(s).H(s)}{(sL + r)} \quad (13)$$

Where $H(s)$ is selected to be as:

$$H(s) = k_{p2} + \frac{k_{i2}}{s} = K_{p2}\left(\frac{1 + T_{i2}s}{T_{i2}s}\right) \quad (14)$$

Using Eq. (12) and Eq. (14) in Eq. (13) gives:

$$G_T(s) = K_{p2}\left(\frac{1 + T_{i2}s}{T_{i2}s}\right)\frac{k}{(1 + sT_a)(1 + sT_d)} \quad (15)$$

Where $k = V_g/r$ and T_a is the output inductor time constant.

It is evident from Eq. (15) that the system has two-time constants: the dominant one is T_a and the minor one is T_d. This makes the optimal modulas technique ideally suitable in designing the PI controller [20]. A zero-pole cancellation is applied when the integral time constant (T_{i2}) is selected to be equal to the dominant time constant (T_a), leaving a system with a second order open loop transfer function. The proportional gain K_{p2} is selected such that the magnitude of the closed loop transfer function $(G_T/(1 + G_T))$ is equal to unity for values of ω as large as possible [15]. Accordingly, K_{p2} and T_{i2} are given as:

$$k_{p2} = \frac{L}{2.V_g\,T_d}, \quad T_{i2} = T_a \quad (16)$$

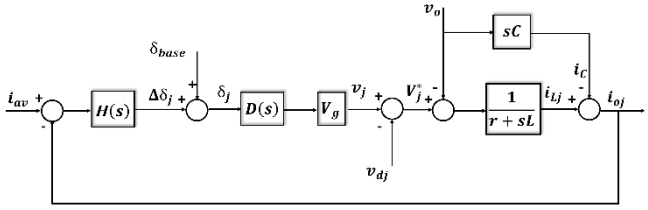

Fig. 5. Control loop for the j[th] converter.

Using the simulation parameters listed in Table 2 at the next section $(L = 3\,mH, r = 0.09\,\Omega, V_g = 30\,V, and\ T_d = 50\,\mu s.)$, the PI compensator gains are $k_{p2} = 1$ and $T_{i2} = 33.33\,ms$ $(k_{i2} = 30)$. The corresponding bode plot of the open loop transfer function is shown in Fig. 6. It is evident that the system phase margin is about 65˚ at a crossover frequency of about (9180 rad/sec) 1461Hz. This is less than one tenth the switching frequency (20kHz) to make the system immune from the switching frequency noise. In contrast, it is high enough to ensure a good dynamic response, as explored in Fig. 7, where the rise time is only about 0.15 ms.

5. Converter Design and Simulation Results

The proposed SAS was designed and a Simulink model constructed. As an illustrative example, a 40 W PV module with the parameters shown in Table 1 was selected to validate the proposal. Figure 8 shows the static V-I curves of the actual PV module. These curves are digitised and stored in lookup tables. Two buck converters were designed such that the output voltage and current can be varied over a wide range, i.e. between open and short circuit points. The inductor (L) and capacitor (C) values were calculated using the following steps:

- The inductor (L) was calculated as [21]:

$$L \geq \frac{V_o(1 - \delta_{min})}{\Delta I_L f_s} \quad (H) \quad (17)$$

Where V_o is the output voltage, δ_{min} is the minimum duty cycle and ΔI_L is the inductor current ripple, which was selected to be twice the minimum load current (I_{omin}). This current ripple value will ensure continuous conduction mode operation (CCM) over all the operating points. However, increasing the inductance value affects the speed of dynamic response. The minimum duty cycle represents the ratio of the output voltage to the maximum input voltage.

- The output capacitor was selected based on the following relationship [21].

$$C \geq \frac{\Delta I_L}{\Delta V_o}\frac{1}{8f_s} \quad (F) \quad (18)$$

Where ΔV_o is the allowable output voltage ripple and f_s is the switching frequency that the simulator operates from the no load point to the short circuit point.

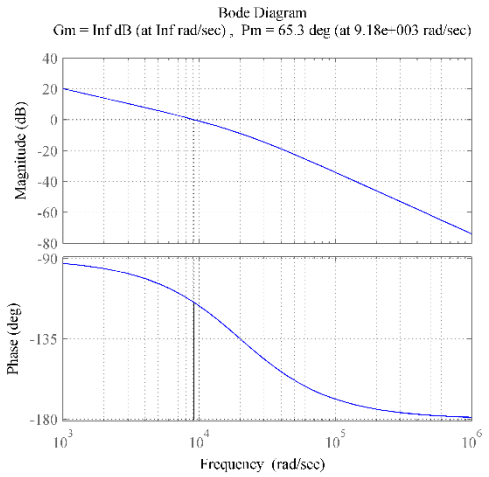

Fig. 6. Bode plot of open loop transfer function (G_T).

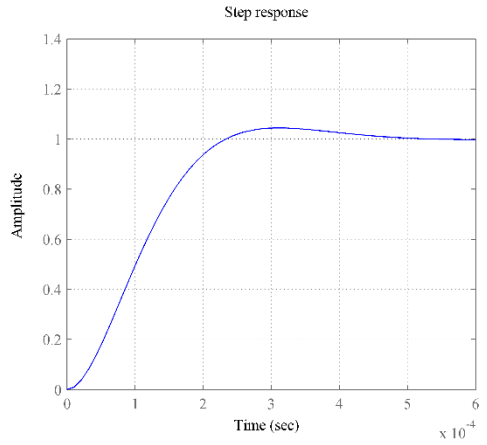

Fig. 7. Step response due to step change in i_{av}.

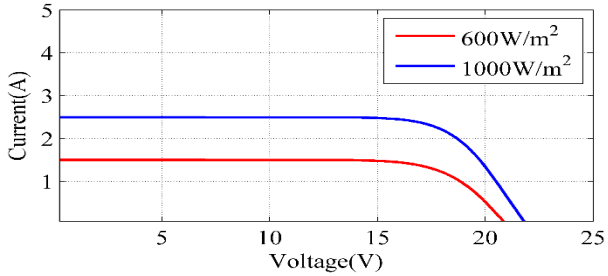

Fig. 8. Static V-I characteristics of the actual PV module at 25 C˚

Table 1. 40W photovoltaic module parameters

Parameter	1000 W/m2	800W/m2
Maximum power	40W	28.8 W
Voltage at Pmax (Vmpp)	17.3 V	15.4 V
Current at Pmax (Impp)	2.31 A	1.85 A
Short circuit current (Isc)	2.54 A	2.06 A
Open circuit voltage (Voc)	21.8 V	19.8 V
Module efficiency	11.4%	-

Figures 9 and 10 show the static V-I and V-P characteristics at 600 W/m^2 at 25 C ˚and 1000 W/m^2 at 25 C˚ obtained from the SAS. These figures reflect the close match between the actual characteristics (Fig. 8) and the output of the SAS. The effect of an abrupt change in irradiance level on the SAS was explored, as shown in Fig. 11. The irradiance level was changed from 600 W/m^2 to 1000 W/m^2 and then attained its original irradiance level. It is clear that the desired characteristics were tracked very well, except for the considerable overshoot. This is insignificant, as the abrupt change in irradiance level is rare and further tuning of the output voltage PI controller can lead to a better response.

Table 2. Buck converter parameters

Output voltage (V_o)	0-25V
$\boldsymbol{\Delta V_o}$	2%
Output current (I_o)	0.1-3A
Input voltage (V_g)	30∓10% V
Switching frequency (f_s)	20 kHz
Inductor with its internal resistor $(L + r)$	3 mH, 0.09Ω
Output capacitor (C)	100 µF

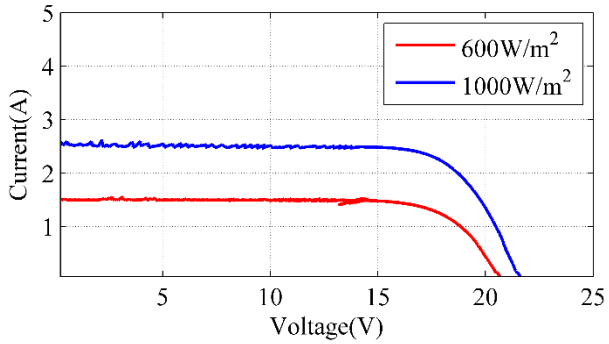

Fig. 9. Static V-I characteristics of the SAS at 25 C˚.

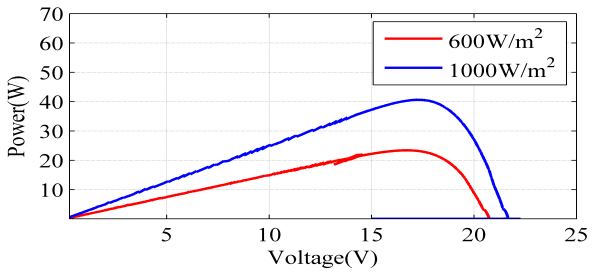

Fig. 10. V-P characteristics of the SAS at 25 C˚.

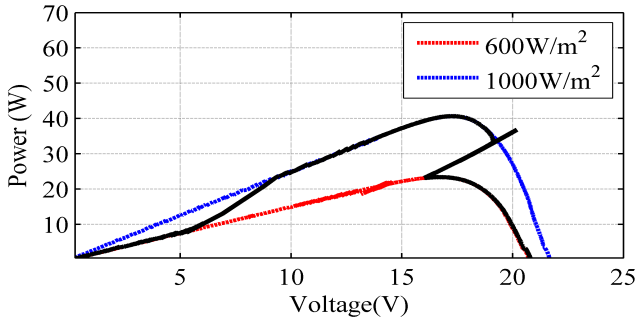

Fig. 11. P-V characteristics during an abrupt change in irradiance level at 25 C°.

To validate the capability of the current distribution controller, which has the effect of virtual resistance emulation in restraining the circulating current between the two converters, the inductor value and dead time of the second converter were intentionally increased by 10%.

At 1000 W/m^2 and 25 C° irradiance and temperature level, the circulating current controller was deactivated. The converters and load current waveforms, referred to as I_1, I_2, and I_o respectively, were explored in Fig.12. There was a clear discrepancy in the converters' current during operation from open circuit point till to the point where the two converters operate in constant current mode. The discrepancy level relative to the total load current reached up to 60%.

After sharing control activation, an excellent current distribution was achieved over all the operating regions, and the two converters shared almost the same current with a discrepancy of not more than 2% (see Fig.13).

6. Conclusions

A solar array simulator with a new modular structure was proposed. The power stage of the simulator was constructed from two parallel-connected buck converters which can easily be controlled and extended to any number of converters since no information is shared between them. This was clearly enhancing the system efficiency and reliability and reducing the voltage and current ripple. Mathematical analysis has been conducted to validate that an excellent current distribution between the parallel converters can be achieved with this proposed control strategy, through increasing the impedance in the circulating current path.

Furthermore, with the results obtained from a Simulink model at different irradiance levels and load variation, the excellent static and dynamic behaviour of the system in terms of V-I curves emulation and current distribution between the converters was confirmed. For two converters having different parameters (inductor values and dead time), the converter current discrepancy relative to the total load current reached up to 60% when no current sharing control was used. This discrepancy was reduced to not more 2% when the proposed sharing controller was activated.

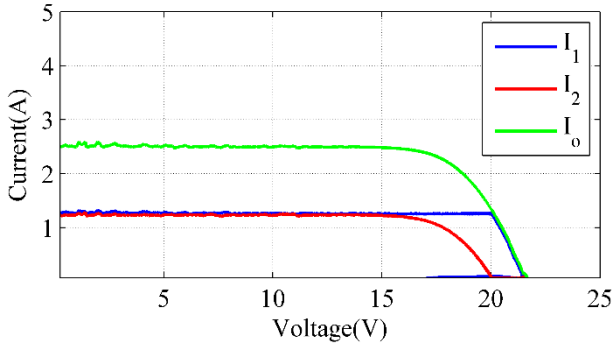

Fig. 12. Converters and load current waveforms when the sharing control was deactivated

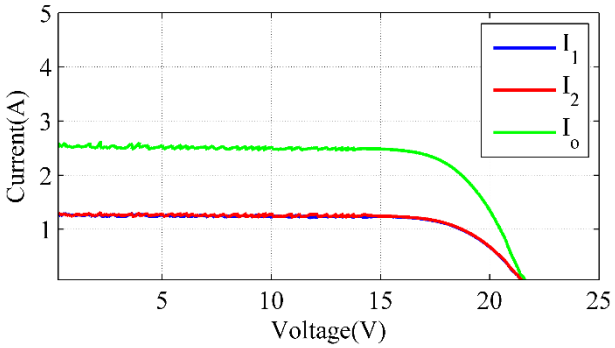

Fig. 13. Converters and load current waveforms when the sharing control was activated.

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