Voltage Sag, Swell and Harmonics Mitigation by Solar Photovoltaic fed ZSI based UPQC

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Received: 10.04.2017 Accepted: 30.07.2017

Abstract- This paper presents a solar photovoltaic (SPV) fed impedance or Z-source inverter (ZSI) based Unified Power Quality Conditioner (UPQC) for the alleviation of power quality events such as voltage sag, swell and harmonics with sudden addition or removal of a nonlinear load. The unit vector template (UVT) control technique is used to produce the reference voltage and current signals to control the operation of SPV fed ZSI-UPQC. A novel hybrid technique is also proposed for optimum maximum power point tracking (MPPT) with the combination of perturbation and observation (P&O) technique and incremental conductance (Inc) technique. The response of SPV fed ZSI-UPQC for mitigation of supply voltage sag, swell and harmonics are investigated and compared with SPV fed voltage source inverter (VSI) based UPQC (VSI-UPQC) and SPV fed current source inverter (CSI) based UPQC (CSI-UPQC).

Keywords Power quality; Voltage sag; UPQC; Photovoltaic; Impedance source inverter.

NOMENCLATURE

V_{m} =Peak Amplitude of the fundamental input voltage I_{SC} = Cell Short circuit current Ua, Ub, Uc =Unit Vector I_{diode} =Diode current V_{dm} =Desired load voltage magnitude V_{pv} =Output voltage of the PV V_{dm} -Desired load voltage magnitude V_{pv} =Output voltage of the PV V_{La} , V^*_{Lb} , V^*_{Lc} =Reference load voltage I_{pv} = Out current of the PV V_{Sav} , V_{Sb} , V_{Sc} =Source voltage R_{S} =Series resistance V^*_{Cabc} =Reference compensator voltage n =Diode identity factor V_{cabc} =Measured compensator voltage V_{t} = terminal voltage I_{Sav} , I^*_{Sb} , I^*_{Sc} =Reference source current n_{S} =No of cells I_{Sav} , I^*_{Sb} , I^*_{Cc} =Reference shunt compensator current n_{P} = No of PV panels in series I_{cav} , I_{Cbv} , I^*_{Cc} =Measured shunt compensator output I_{dr} =Diode reverse saturation current I_{pc} =Photovoltaic current I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{dr} =Diode reverse current I_{pc} =Photovoltaic current I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{sh} =Short circuit current I_{pc} =Photovoltaic current I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{sh} =Short circuit current I_{pc} =Reference shunt compensator output I_{sh} =Short circuit current	<i>k</i> =Gain	Tref=Cell temperature
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$ I_{pc} = Photovoltaic current \\ g_{K} = Solar irradiation $ $ I_{sh} = Short circuit current \\ a = Transformation ratio $	I_{Ca} , I_{Cb} , I_{Cc} =Measured shunt compensator output	I _{dr} =Diode reverse saturation current
g _K =Solar irradiation a=Transformation ratio	current	I _{rs} =Diode reverse current
	I _{pc} =Photovoltaic current	I _{sh} =Short circuit current
	g_{K} =Solar irradiation	a=Transformation ratio
To=Operating temperature <u>t=time</u>	To=Operating temperature	t=time

V_S=Supply voltage V_{inj}=Injected voltage V_{load}=Load voltage

1. Introduction

Today, many researchers have given their spotlight on voltage and current quality. Among all power quality perturbations, sags, swells and harmonics represent the most common, frequent and vintage power quality degrading factors in these days power system [1-4]. UPQC is one of the key custom power devices (CPDs) which can compensate voltage and current distortions simultaneously [5-7]. Generally, the UPQCs consist of VSI [8-10], CSI [11] and ZSI for the alleviation of voltage sags, swells, and harmonics. The VSI is buck (step-down) type so the maximum output voltage is limited by DC link voltage. A condition of shoot through would appear and damage the IGBT switches if upper and lower switches of each leg of VSI fired on at the same time. The CSI is a boost type so the voltage at output level is greater than the DC voltage level. One of the big problems in CSI is that the open circuit across DC inductor would appear and damage the insulated gate bipolar transistor (IGBT) switches if any instant of time at least of one upper and lower switches cannot be fired on and keep it on. The demerits of traditional converters such as VSI and CSI are discussed [12, 13]. Therefore the application of ZSI based UPQC technology seems very promising. ZSI has both step-down and step-up facility. Due to the presence of this unique character it permits converters to be worked in the shoot-through condition. Unlike a VSI and CSI, the shoot-through state is not harmful and actually has been utilized in ZSI. A great amount of research has been carried out in ZSI and its topologies. Looking at the various advantages of ZSI over traditional converters it has decided to study photovoltaic fed ZSI based UPQC (PV-ZSI-UPQC) and compare the performance with that of PV-VSI-UPQC and PV-CSI-UPQC topologies. The fossil fuels are the main source of fulfilled worldwide energy demand, but at the same time due to increased price, environmental pollution, and global warming have made it compulsory used renewable energy sources. Renewable energy such as solar photovoltaic seems to have an increasing importance because it has several advantages, such as it has no noise or moving parts, and it does not need any means of fuel. It has low maintenance cost and it is environmental friendly [8, 9, 16]. Despite these advantages, the I-V characteristics of a PV panel are extremely nonlinear and alter with irradiation and temperature. There is a solo working point called maximum power point (MPP) on the I-V curve of the PV panel. The PV panel produces its maximum output power and operates with a maximum efficiency under certain irradiance and temperature conditions. Therefore, MPPT techniques are needed to maintain an operating point of the PV panel at its MPPT [17-20]. In this work, a novel hybrid technique is proposed for optimum MPPT with the combination of P&O and InC techniques. The performance of PV fed UPQCs depends on the control algorithm used for reference voltage and current calculation. For the generation of a reference voltage and current signals currently large numbers of

V_C= Capacitor voltage I_L=Inductor current

control techniques are used. The commonly adopted theories are p-q theory, synchronous reference frame (SRF) theory [1, 21-23], Fuzzy Logic Controller [24-26], Resistive optimization technique [20] and Neural Networks Technique [28-30]. This paper presents, a solar photo-voltaic (SPV) fed impedance or Z-source inverter based Unified Power Quality Conditioner (ZSI-UPQC) for the mitigation of power quality issues namely voltage sags, swells and harmonics and compare the results with conventional SPV fed VSI based UPQC (VSI-UPQC and) and SPV fed CSI based UPQC (CSI-UPQC). The Unit Vector Template (UVT) control strategy is used to control the operation of PV fed UPQCs. Extensive MATLAB/Simulink studies are performed for mitigation of short duration serious voltage sags, swells and source current and load voltage harmonics. Based on the simulation results, the detailed comparative analysis is also done.

2. Configuration of UPQC

Figure 1 shows the power circuit configurations of the PV-ZSI-UPQC. The power circuit of UPQC consists of two six leg and impedance source inverters joined back to back by a common dc-link produced by solar photovoltaic with low step-up converter and a UVT control. The series part of PV fed UPQC is used to mitigate the destructive voltage disturbances namely voltage sags, swells, fluctuations. Similarly, the shunt part of PV fed UPQC eliminates harmonics and contributes reactive power compensation.

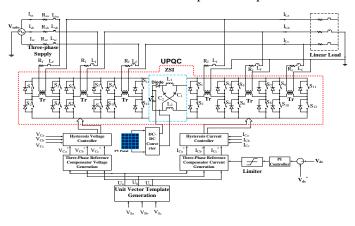


Fig. 1. Schematic diagram of the proposed PV fed ZSI-UPQC

3. Control Methodology

The performance of PV fed UPQC system totally depends on its control technique for generation of a reference voltage and current signals.

3.1. UVT Control Technique for Series Active Power Filter

Figure 2 shows the Unit Vector Template (UVT) based control algorithm of series part of UPQC for the production of reference voltages. The distorted supply voltages are measured and multiplied by the gain K, which is equal to $(1/V_m)$. Where V_m is the peak amplitude of fundamental input voltage is calculated by using equation (1) [14].

$$V_m = \sqrt{\left(2/3\right) \left(V_{Sa}^2 + V_{Sb}^2 + V_{Sc}^2\right)} \tag{1}$$

The obtained supply voltages are passed to phase locked loop (PLL). The main function of PLL is to maintain the synchronization with supply voltage and produce a unit vectors (U_a, U_b, U_c) is obtained by using equation (2).

$$\begin{aligned}
 U_a &= Sin(\omega t) \\
 U_b &= Sin(\omega t - 2\pi/3) \\
 U_c &= Sin(\omega t + 2\pi/3)
 \end{aligned}$$
(2)

The reference load voltage waveforms are produced by multiplying the computed three in phase unit vector template with the desired load voltage magnitude V_{dm} is given in equation (3).

$$\begin{bmatrix} V_{La}^* \\ V_{Lb}^* \\ V_{Lc}^* \end{bmatrix} = \begin{bmatrix} V_{dm} \end{bmatrix} \begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix}$$
(3)

The obtained reference load voltages $(V_{La}^*, V_{Lb}^*, V_{Lc}^*)$ are compared with three-phase source voltages (V_{Sa}, V_{Sb}, V_{Sc}) and multiplied with 'a', where 'a' is the transformation ratio of a series transformer and produces reference compensator voltage (V_{Cabc}^*) . The reference compensator voltage and measured series compensator output voltage (V_{Cabc}) are then given to hysteresis voltage controller to produce the firing signals.

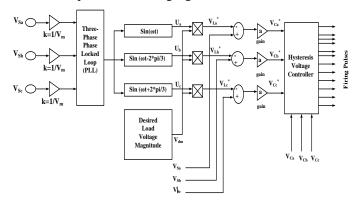


Fig. 2. UVT control technique for Series Active Power

3.2. UVT Control Technique for Shunt Active Power Filter

The working of UVT strategy for shunt active power filter is similar to the series active power filter but in shunt active power filter additionally compares the measured dclink voltage with reference dc-link voltage as shown in figure 3. The obtained error is given as input to a proportional integral controller and generates an output signal which is multiplied with UVGT and produces reference source current waveforms is given in equation (4).

$$\begin{bmatrix} I_{Sa}^{*} \\ I_{Sb}^{*} \\ I_{Sc}^{*} \end{bmatrix} = \begin{bmatrix} I_{m} \end{bmatrix} \begin{bmatrix} U_{a} \\ U_{b} \\ U_{c} \end{bmatrix}$$
(4)

The obtained reference supply current signals are compared with supply current signals and generates reference output current of shunt compensator $(I_{Ca}^*, I_{Cb}^*, I_{Cc}^*)$ and these signals are given to hysteresis current controller along with the measured shunt- compensator output currents (I_{Ca}, I_{Cb}, I_{Cc}) [22].

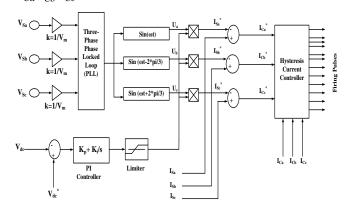


Fig. 3. UVT control technique for shunt active power

filter

4. Mathematical Modeling of Solar Photovoltaic (SPV)

Photovoltaic system presents an alternative solution for electricity supply especially for remote locations because of low maintenance requirement, high reliability, long life, and stability with un-rotating units [13]. The basic diagram for modeling the solar PV system is depicted in figure 4.

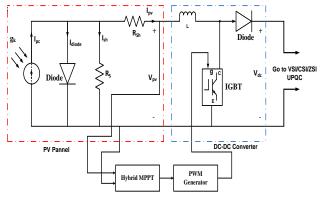


Fig. 4. PV modeling with step-up dc-dc converter and hybrid MPPT algorithm

The basic equation of the PV cell is defined in the equation (5).

$$I_{PV} = I_{pc}n_p - I_{diode} - I_{sh}$$
⁽⁵⁾

Where I_{PC} is a photocurrent mainly depends up the solar irradiation and cells working temperature, which is described in the equation (6).

$$I_{PC} = g_K \left[I_{SC} + K_i \left(T_o - T_{ref} \right) \right] \tag{6}$$

Where g_K is a solar irradiation in kW/m², T_o is the cell operating temperature, T_{ref} is the cell temperature at 25°C and I_{SC} is the cells short circuit current. The current following to the diode is represented by equation (7).

$$I_{diode} = \begin{bmatrix} e^{\left(\frac{V_{PV} + I_{PV}R_{S}}{nV_{t}Cn_{S}}\right)} - 1 \end{bmatrix} I_{dr}n_{P}$$
(7)

Where I_{diode} is the diode current, V_{PV} is the output voltage of the PV panel, I_{PV} is the output current of the PV panel, R_S is the series resistance, n is the diode identity factor, V_t is the terminal voltage, C is the number of cells in PV panel, n_S is the number of PV panels in series, n_P is the number of PV panels in parallel and I_{dr} is the diode reverse saturation current. The diode reverse saturation current is defined in the equation (8).

$$I_{dr} = I_{rs} \left(\frac{T_o}{T_{ref}}\right)^3 e^{\left[\left(\frac{qE_b}{nk}\right)\left(\frac{1}{T_o} - \frac{1}{T_{ref}}\right)\right]}$$
(8)

Where I_{rs} is the diode reverse current at operating temperature, q is the charge of an electron, E_b is the bandgap energy of the cell and k is the Boltzmann's constant. The shunt current I_{sh} obtained from the equivalent circuit of PV module is given in the equation (9).

$$I_{sh} = \left(\frac{V_{PV} + I_{PV}R_S}{R_P}\right) \tag{9}$$

After putting the values of I_{diode} and I_{sh} from equations (7) and (9) in equation (5), we obtained equation (10).

$$I_{PV} = I_{pc}n_p - \left(e^{\left(\frac{V_{PV} + I_{PV}R_S}{nV_tCn_s}\right)} - 1\right)I_{dr}n_p - \left(\frac{V_{PV} + I_{PV}R_S}{R_p}\right)(10)$$

5. Maximum Power Point Tracking (MPPT) Method

The MPPT is the heart of the solar PV system. In this paper, a hybrid MPPT algorithm with a combination of P&O and InC with a dc-dc converter is integrated to measure the optimum maximum power point from the solar system.

5.1 Proposed Hybrid MPPT Algorithm

Flow chart of the proposed hybrid MPPT technique is highlighted in figure 5. The objective of this proposed technique is to obtain the combine advantages of P&O and InC techniques. This technique is used to calculate the output power after measuring the voltage and current from the solar system. Now it compares the power with a previous value of power by finding the change in power. The proposed algorithm checks whether $\Delta I/\Delta V$ is greater than, less than or equal to -I/V and gives its decision whether to increase or decrease the terminal voltage. Figure 6 depictes the MATLAB/Simulink model of the proposed hybrid MPPT technique.

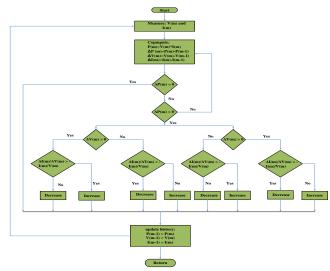


Fig. 5 Flowchart of the Proposed Hybrid MPPT Technique

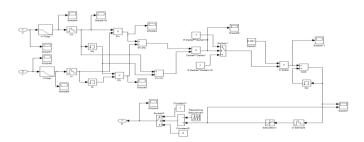


Fig. 6. MATLAB/Simulink model of the proposed Hybrid MPPT Technique

6. Simulation Results and Discussion

To show the effectiveness of the PV fed ZSI based UPQC with its associated UVT control technique and the

power circuit given in figure 1 has been established with MATLAB/Simulink software. The simulation parameters of the system shown in table 1. To obtain the optimal maximum power point, the new hybrid scheme with the combination of P&O and InC technique has been used. The PV array with low step-up DC-DC converter gives greater output voltage as exposed in figure 7. Figure 8(a-c) shows that the proposed technique is more useful in extracting maximum power point (MPP =152 W) from a solar PV system compared to a maximum power point (MPP =151W) in a case of P&O technique and maximum power point (MPP=151.58 W) in a case of incremental conductance method. The most important goal of this section is to estimate the performance of the proposed PV fed ZSI-UPQC in comparison with that of traditional PV fed VSI-UPQC and CSI-UPQC for the alleviation of power quality events such as supply voltage sags, swells and supply current as well as load voltage harmonics.

Parameters	Values		
Supply Voltage (Vs)	380 V		
Frequency (f)	50 Hz		
Supply Resistence (Rs)	0.05 Ω		
Supply Inductance (Ls)	3.5 µH		
I 's set as 1	Active Power (P)= 5kW		
Linear Load	Inductive reactive power $(Q_L) = 10 \text{ kVAR}$		
Nonlinear Load	Diode rectifier, Rd= 10 Ω, Ld= 3μH		
Injection Transformer	240/120 V		
DC-bus Voltage (Vdc)	150 V		
	$V_{OC} = 40 \text{ V}$		
	$I_{SC} = 5.8 \text{ A}$		
	No of solar cells (C) = 36		
	Pmax = 152 W		
	$V_{MPP} = 35.5 V$		
	$I_{MPP} = 4.28 \text{ A}$		
Solar module	Diode identity factor (n) = 1		
	$Rs = 0.18 \Omega$		
	$Rp = 360.002 \ \Omega$		
Step-up DC-DC	Inductance= 0.01H		
converter	İnput/output voltage= 45/150 V		

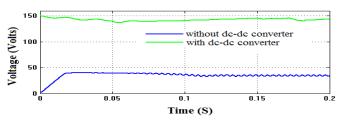


Fig. 7. PV array output voltages without DC-DC converter and with DC-DC converter

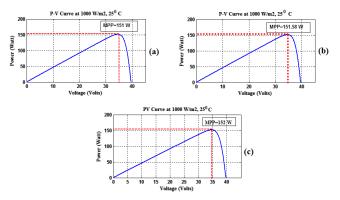


Fig. 8. Comparison of MPPT (a) Perturbation and Observation (b) Incremental Conductance and (c) Proposed Hybrid Technique

6.1. Performance of PV fed VSI-UPQC for mitigation of voltage sags

Due to sudden switching a nonlinear load, a three-phase voltage sag occurs in the supply terminals of the distribution network from t=0.05s to t= 0.15s for fourteen cycles of the supply voltage. For voltage sag of 15%, the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}) and dc-link capacitor voltage (V_{dc}) are observed and depicted in figure 9(a-e). For a period of voltage sag only PV fed VSI-UPQC is connected to the system and provide a correct amount of missing voltage quickly as shown in figure 9c and minimize the effect of serious voltage sag so that load voltage become acceptable level as highlighted in figure 9d. Figure 9e shows the variation of dc-link capacitor voltage during sudden switching a nonlinear load.

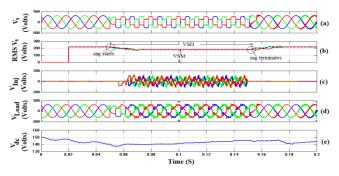


Fig. 9. Simulation results of VSI-UPQC (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) DC-link capacitor voltage

6.2. Performance of PV fed VSI-UPQC for mitigation of voltage swells

Due to sudden switching a capacitor bank, a threephase voltage swell occurs in the supply terminals of the distribution network from t=0.05s to t= 0.15s for fourteen cycles of the supply voltage. For voltage swell of 20%, the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}) and dc-link capacitor voltage (V_{dc}) are observed and depicted in figure 10(a-e). For a period of voltage swell only PV fed VSI-UPQC is connected to the system and provide a correct amount of missing voltage quickly as shown in figure 10c and minimize the effect of serious voltage swell so that load voltage become acceptable level as highlighted in figure 10d.

The behavior of DC-link voltage during voltage swell event

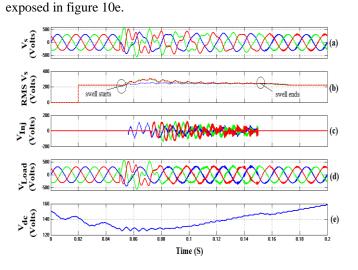


Fig. 10 Simulation results of VSI-UPQC under 20% voltage swell (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) DC-link Capacitor Voltage

6.3. Performance of PV fed CSI-UPQC for mitigation of voltage sags

Figure 11(a-e) shows the compensation effect of PV fed CSI-UPQC during voltage sag condition. For voltage sag of magnitude 15%, the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}) and dc-link inductor current (I_{dc}) are noted and highlighted in figure 11(a-e). The solar PV fed CSI-UPQC comes into action for a duration of under voltage (sag) event and produces accurate voltage magnitude with proper polarity and introduce into the distribution network. Due to this load voltage becomes insensitive to voltage sags as shown in figure 11d. Figure 11e demonstrates the variation of dc-link inductor current during sudden switching a nonlinear load.

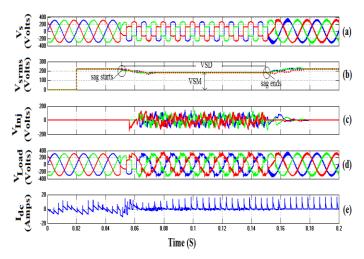


Fig. 11. Simulation results of CSI-UPQC (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) DC-link inductor current

6.4. Performance of PV fed CSI-UPQC for mitigation of voltage swells

Figure 12(a-e) shows the compensation effect of PV fed CSI-UPQC during voltage swell condition. For voltage swell of magnitude 20%, the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}) and dc-link inductor current (I_{dc}) are noted and highlighted in figure 12(a-e). The solar PV fed CSI-UPQC comes into action for a duration of voltage swell event and produces accurate voltage magnitude with proper polarity and introduce into the distribution network. Due to this load voltage becomes insensitive to voltage swells as shown in figure 12d. Figure 12e demonstrates the variation of dc-link inductor current during sudden switching a capacitor bank.

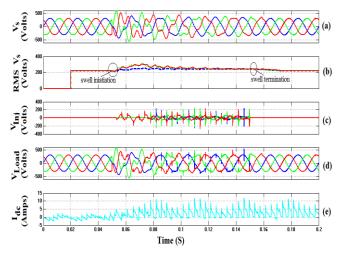


Fig.12 Simulation results of CSI-UPQC under 20% voltage swell (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) DC-link Inductor Current

6.5 Performance of PV fed ZSI-UPQC for mitigation of voltage sags

Figure 13(a-f) highlights the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}), voltage across capacitor (V_C) and current in the inductor (I_L) of PV fed ZSI-UPQC during voltage sag condition. A three-phase balanced voltage sag of magnitude 15% encounters in the interval of 0.05 s \leq t \geq 0.15 s for fourteen cycles of the supply voltage as shown in figures 13a and b. During voltage sag condition source voltage decreases and at t= 0.05s to t= 0.15s the PV fed ZSI-UPQC joined to the system and produces a right magnitude of compensation voltage with correct polarity and eliminate the destructive voltage sags as shown in figure 13c. As a result load voltage insensitive to supply voltage disturbances as shown in figure 13d. The variation of capacitor voltage and inductor current of PV fed ZSI-UPQC are highlighted in figures 13e and f.

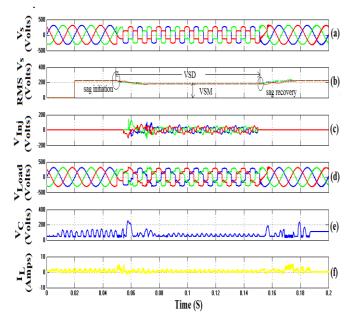


Fig. 13. Simulation results of ZSI-UPQC (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) Capacitor voltage and (f) Inductor current

6.6 Performance of PV fed ZSI-UPQC for mitigation of voltage swells

Compensated Figure 14(a-f) highlights the supply voltage (V_S), RMS supply voltage (RMS V_S), injected voltage (V_{Inj}), load voltage (V_{Load}), voltage across capacitor (V_C) and current in the inductor (I_L) of PV fed ZSI-UPQC during voltage swell condition. A three-phase balanced voltage swell of magnitude 20% encounters in the interval of 0.05 s \leq t \geq 0.15 s for fourteen cycles of the supply voltage as shown in figures 14a and b. During voltage swell condition source voltage increases and at t= 0.05s to t= 0.15s the PV fed ZSI-UPQC joined to the system

and produces a right magnitude of compensation voltage with correct polarity and eliminate the destructive voltage swells as shown in figure 14c. As a result load voltage insensitive to supply voltage disturbances as shown in figure 14d. The variation of capacitor voltage and inductor current of PV fed ZSI-UPQC are highlighted in figures 14e and f.

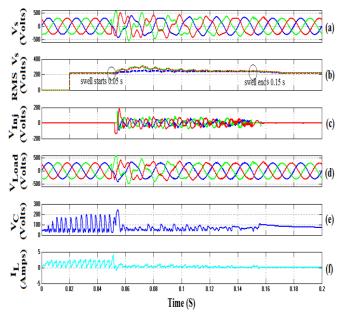
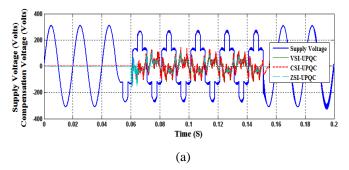


Fig. 14 Simulation results of ZSI-UPQC under 20% voltage swell (a) supply voltage (b) RMS supply voltage (c) Injected voltage (d) Load voltage and (e) Capacitor voltage and (f) Inductor current

7. Comparative analysis of PV fed VSI, CSI and ZSI based UPQCs

Compensated Compensated and uncompensated load voltages under voltage sag and swell condition are depicted in figures 15 and 16. Initially, PV fed VSI, CSI, and ZSI based UPQCs are not connected to the system so system experiences voltage sag of a magnitude of 15% (46.5V) and voltage swell of magnitude 20% (62V) of the supply voltage.

During voltage sag event PV fed VSI-UPQC injects the voltage of 100 volts, CSI-UPQC injects the voltage of 134 volts and proposed ZSI-UPQC injects the voltage of 50 volts as shown in figure 15a. The solar PV fed proposed ZSI-UPQC generates the appropriate amount of missing voltage compared to VSI-UPQC and CSI-UPQC. As a result load voltage becomes sinusoidal as shown in figure 15b.



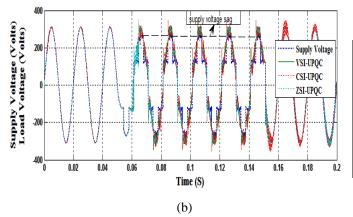


Fig. 15. Comparison of VSI, CSI and ZSI based UPQCs under voltage sag (a) Injected voltages and (b) Load voltages

During voltage swell event PV fed VSI-UPQC injects the voltage of 120V, CSI-UPQC injects the voltage of 200V and proposed ZSI-UPQC injects the voltage of 65V as shown in figure 16a. The PV fed proposed ZSI-UPQC shows the superior performance to generate the appropriate amount of injected voltage compared to VSI-UPQC and CSI-UPQC. As a result, load voltage becomes acceptable level as shown in figure 16b.

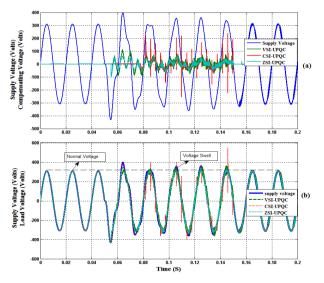


Fig. 16 Comparison of VSI, CSI and ZSI based UPQCs under voltage swell (a) Injected voltages and (b) Load voltages

The performance of load voltage and source current harmonics filtering of PV fed-UPQCs during load switching condition is illustrated in Tables 2-3.

During load switching the source current THD_i without UPQCs is obtained as 7.28%, while, THD_i of source current after compensation is found to be 1.67%, 1.66% and 160% in the case of VSI-UPQC, CSI-UPQC and ZSI-UPQC respectively as shown in Table 2. Thus, 78.02% reduction in THD_i has been achieved using ZSI-UPQC compared to 77.06% reduction in THD_i of VSI-UPQC and 77.20% reduction in THD_i of CSI-UPQC.

Table 2. Supply current harmonics THD_i of VSI, CSI and proposed ZSI UPQCs

	VSI-UPQC		CSI-UPQC		Proposed ZSI- UPQC	
Before compe nsation	With VSI- UPQ C (%)	Impro vemen t in THD _i (%)	With VSI- UPQC (%)	Improve ment in THD _i (%)	With VSI- UPQ C (%)	Improve ment in THDi (%)
7.28	1.67	77.06	1.66	77.20	1.60	78.02

The THD_v of load voltage measured without VSI, CSI, and ZSI based UPQCs is observed as 25.96%, whereas the same is observed as 1.72% in the presence of VSI-UPQC, 4.20% in the case of CSI-UPQC and 0.07% in the presence of ZSI-UPQC as shown in Table 3. Thus, 93.37%, 83.82% and 99.73% reduction in THD_v have been achieved. The ZSI-UPQC shows the superior performance of reduction in THD_v in compare to VSI-UPQC and CSI-UPQC.

Table 3. Load voltage harmonics THD_{s} of VSI, CSI and proposed ZSI UPQCs

Befor	VSI-	VSI-UPQC		CSI-UPQC		Proposed ZSI- UPQC	
e comp ensati on	With VSI- UPQ C (%)	Impro vemen t in THD _i (%)	With VSI- UPQC (%)	Improv ement in THD _i (%)	With VSI- UPQC (%)	Improv ement in THDi (%)	
25.96	1.72	93.37	4.20	83.82	0.07	99.73	

8. Conclusion

This paper describes, a solar photovoltaic (PV) fed ZSI-UPQC for the minimization of sags, swells and harmonics with addition or removal of the nonlinear load. A novel hybrid technique with the combination of P&O and InC technique is also proposed. The proposed hybrid technique shows the superior performance to produce maximum power output compared to P&O and InC techniques. The proposed hybrid technique also controls the power loss by controlling the oscillations around the MPP. The PV fed UPQC is responsible for the fast and accurate production of injecting voltage and injects it into the system for compensation of supply voltage disturbances such as voltage sags and swells. The obtained simulation results show that proposed SPV fed ZSI-UPQC injects the appropriate amount of three-phase injecting voltage compared to SPV fed VSI and CSI based UPQCs. The simulation results also prove that the proposed SPV fed ZSI-UPQC shows a superior capability to annihilate the source current and load voltage harmonics compared to SPV fed VSI-UPQC and CSI-UPQC.

Acknowledgements

The authors are thankful to All India Council of Technical Education (AICTE), Ministry of Human

Resources Development (MHRD), and Government of India for providing financial assistance to do the research work under Technical Quality Improvement Program-II (TQIP-II).

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