Cascaded Multilevel Inverter with Minimum Number of Conducting Switches and Using Capacitor Compensation

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Abstract- This paper presents the design and implementation of an improved cascaded multilevel inverter topology with symmetrical DC source with minimum number of switching and minimum conducting switches during operation The proposes new topology is designed as a stand-alone system and simulated using resistive and inductive loads. One drawback of the others topology is the occurrence of voltage surges in the inductive load due to the emf effect. By using a capacitor on the dc bus as a compensation, the emf effect can be minimized. The size of the capacitor used should be proportional to the reactive power of the load. The proposed new topology is more efficient in use of switching components, conducting switches and can overcome inductive loads. It can generate 21 level with 14 switches needed and only 3 conducting switches during operation. The value of THDv and THDi from the proposed new topology is 3.76% and 0.93%, it varies depending on the value of the load received.

Keywords: Symmetrical source, multilevel inverter, minimum switching devices, capacitor compensation

1. Introduction

Inverter is the main components to convert direct current electrical energy (DC / Direct Current) into an alternating current electrical energy (AC / Alternating Current) in order to supply electricity to an AC load [1]. Inverters play an important role in human life because they can be used as variable speed motors, inverter air conditioners, uninterruptible power supply (UPS), induction cookers, DC power transmission (HVDC / High Voltage Direct Current), electric vehicles, active power filters and can be implemented for renewable energy power plants [2].

Basically, there are two types of inverter technology, namely Voltage Source Inverter (VSI) and Current Source Inverter (CSI). Voltage Source Inverter (VSI) can be classified into two-level inverter and multilevel inverter (MLI) [3]. MLI technology was first introduced by Nabae in 1981 by making a three-level inverter that utilizes the neutral point of a direct current (DC) voltage source [4]. The most important benefit of MLIs are to decrease the *dv/dt* stress on switches and to generate increased output levels [5][6]. Improvements in the design of the multilevel inverter (MLI) are still being made until now.

Multilevel inverters have been widely used in academic discussions on the technique of converting DC waveforms to AC waves because they have several advantages, including the ladder waveform can display a better harmonic profile and the saturation voltage on the semiconductor component is smaller when compared to a fully operational voltage [2][4].

The number of levels designed will affect the quality of the resulting output waveform, where the MLI output will approach a sinusoidal wave and the percentage of total harmonic distortion (THD) will be smaller if the number of levels designed is increasing [7]. Based on the IEEE STD 519 2014 standard, it is stated that the limit of the THD value for bus voltages below 1 kV at the point of common coupling does not exceed 8% [8]. The total output voltage of a multilevel inverter is the sum of the voltages at the

designed level source. To achieve a certain voltage value at the output, we must provide the sum of the level voltage source equal to the output voltage.

The main disadvantage of an MLI is the large number of switching components required in each design. They will increase the size of the inverter circuit and increase the cost. Power losses in the connected switching components will also increase (usually in the form of heat) and there will be a reduction in voltage at the output terminals due to the accumulation of voltage drops that pass through quite a lot of switching components [9][10].

There have been many studies on topological design and performance analysis of multilevel inverters as discussed in research [2]. Researchers have designed various MLI topologies which usually aim to minimize the use of switching components with low THD values but have not considered multilevel inverters with high power performance. MLI can be said to have high power performance if the quality of the output waveform is maintained properly even though it is burdened with various types of loads. In research [9] has designed an inverter topology with low THD value and it is able to overcome inductive resistive loads (RL Loads) so as to produce a multilevel inverter with high power performance. But the design [9] uses more switching components because these components are used as reverse current switches, output voltage level switches and H-Bridge switches.

The author argues that the design given in research [9] can still be simplified again by substituting the MOSFET switching circuit used as a reverse current switch into a capacitor circuit. So that the use of switching components can be minimized by only using MOSFETs as output voltage level switches and H-Bridge switches. The proposed new topology is designed as an alternative inverter model that can be applied to stand alone systems with resistive (R) and inductive (L) loads, for example as an inverter in a stand-alone PV system. By adding a capacitor will produce a high-performance multilevel inverter with low THD value and minimum switching component used. The capacitor can minimize the reactive power generated by the induced load. Reducing THD and decreasing conduction switching losses will improve power quality [11].

2. Principle of Operation, Switching Degree and Topology

2.1 Principle of Operation

The main purpose of an inverter is to produce an AC (Alternating Current) output wave from a DC (Direct Current) source [10]. Several methods can be applied in designing an inverter, one of which is the Pulse Width Modulation (PWM) method so that it can produce an AC waveform with adjustable frequency and amplitude inverter [12]. Multilevel inverter (MLI) works by utilizing DC voltage from several levels to produce an output wave that is close to a sinusoidal wave shaped like a ladder wave [13]. By adding more DC levels, the total harmonic distortion will decrease (closer to zero) and the resulting output wave will be closer to a sinusoidal wave [14]. The output voltage can be interpreted as the voltage across the output terminal of the inverter to the ground point [10].

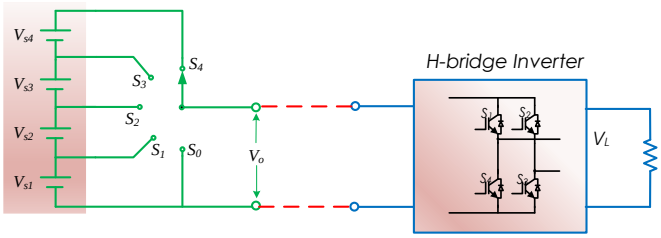
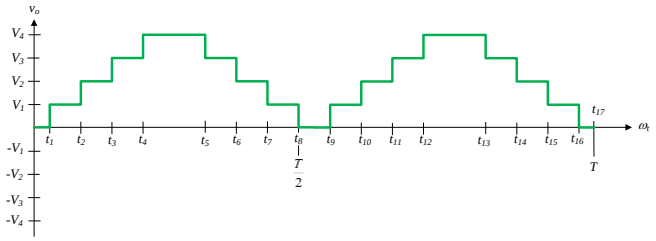
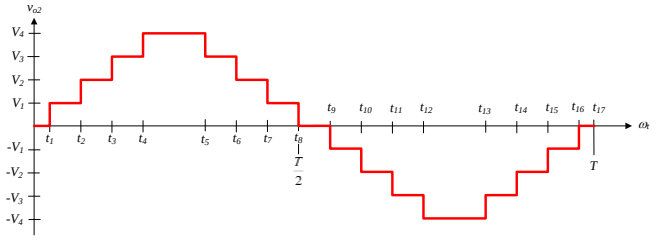


Fig. 1. MLI basic concept with H-Bridge Inverter.



(a)



(b)

Fig. 2. MLI output waveform.
(a) Output Voltage before H-Bridge Inverter. (b) Output Voltage after H-Bridge Inverter

The basic concept of a multilevel inverter circuit can be seen in fig.1 where the circuit requires a switch to select the sum of the voltage levels to be connected to the load. While the output wave can be seen in fig.2. Some semiconductor components such as Metal Oxide Field Effect Transistor (MOSFET), Bipolar Junction Transistor (BJT), Insulated Gate Bipolar Junction Transistor (IGBT), Static Induction Transistor (SIT), and Gate Turn Off thyristor (GTO) and Thyristors such as Silicon Controlled Rectifiers (SCR) can be used as a switching component [10][15][16].

2.2 Switching Degree of The Proposed Cascaded Multilevel Inverter

Graphical method of sine wave is used to determine switching degree of the proposed new cascaded multilevel inverter. A full sine wave in one period is divided into 4 quadrants (see fig.3), they are quadrant 1 (0° to 90° or 0 to $\frac{T}{4}$), quadrant 2 (90° to 180° or $\frac{T}{4}$ to $\frac{T}{2}$), quadrant 3 (180° to 270° or $\frac{T}{2}$ to $\frac{3T}{4}$) and quadrant 4 (270° to 360° or $\frac{3T}{4}$ to T).

Each quadrant uses different equations such as equations 1, 2, 3 and 4.

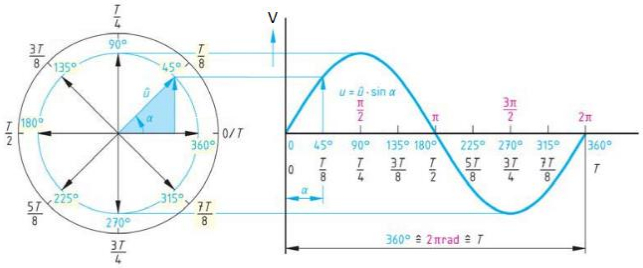


Fig 3. Quadrant division of a one-period sine wave.

Quadrant 1

$$t_n = Sin^{-1}\left(\left(\sum_{n=1}^{n} V_{S(n)} - \frac{V_S}{2}\right) \div V_t\right) \quad (1)$$

Quadrant 2

$$t_n = 180 - Sin^{-1}\left(\left(\sum_{n=1}^{n} V_{S(n)} - \frac{V_S}{2}\right) \div V_t\right) \quad (2)$$

Quadrant 3

$$t_n = 180 + Sin^{-1}\left(\left(\sum_{n=1}^{n} V_{S(n)} - \frac{V_S}{2}\right) \div V_t\right) \quad (3)$$

Quadrant 4

$$t_n = 360 - Sin^{-1}\left(\left(\sum_{n=1}^{n} V_{S(n)} - \frac{V_S}{2}\right) \div V_t\right) \quad (4)$$

t_n = time in level n

$V_{S(n)}$ = DC Souce voltage level n

V_t = Total DC Source Voltage

2.3 Topology of The Proposed Cascaded Multilevel Inverter

The percentage of total harmonic distortion (THD) will be smaller when the number of levels designed is increasing [17][11]. Meanwhile, increasing the number of levels will increase the number of switching component usage and switching component losses will also be higher [18]. The multilevel inverter design consists of forward switching and reverse switching. Reverse switching serves to eliminate the reactive power generated by the induced load. By installing a compensator circuit, the use of MOSFETs as reverse switching can be eliminated and the number of switching components used is reduced.

The topology in this paper is bases on [9][3] to allow RL loads. The simulation using 10 DC source (each 18 Vdc) to produce 21 level with minimum the number of switches needed, minimum conducting switch at any time operation and produce 1 phase AC output.

Topology of cascaded multilevel inverter for RL Loads [9] places the reverse current switches parallelly with the diodes to overcome RL loads (see fig.4). The topology with n cells will produce 2n+1 output voltage levels, using 2n+6 switches needed and 4 switches will conduct at any time operation. The disadvantages of topology are too many switches needed and too many conducting switches in operation.

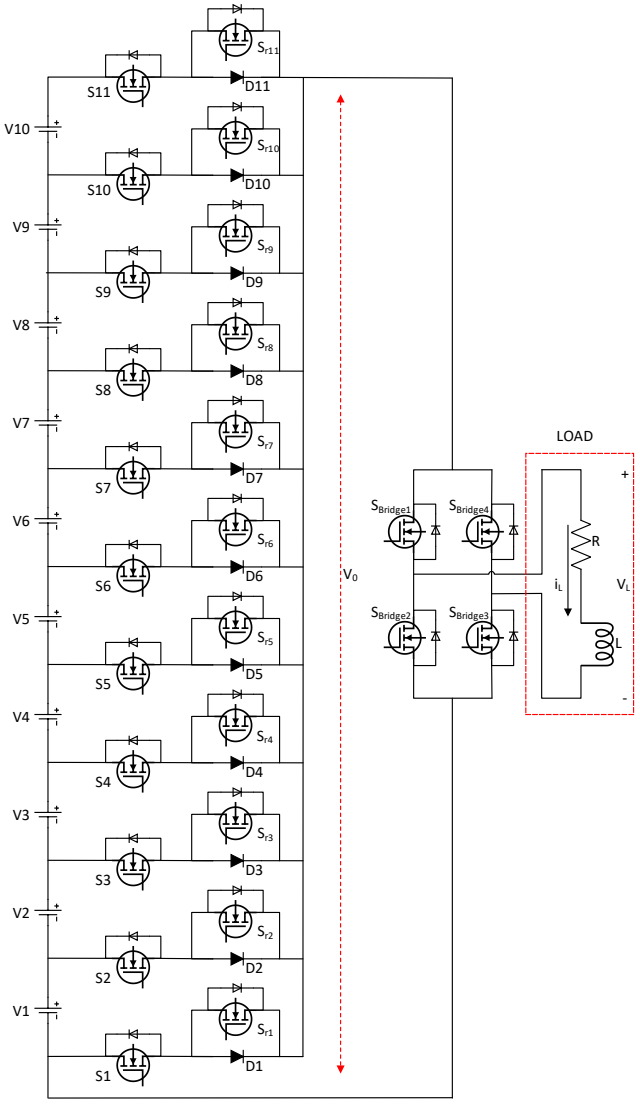


Fig. 4. Cascaded multilevel inverter topology 21 level for RL loads [9].

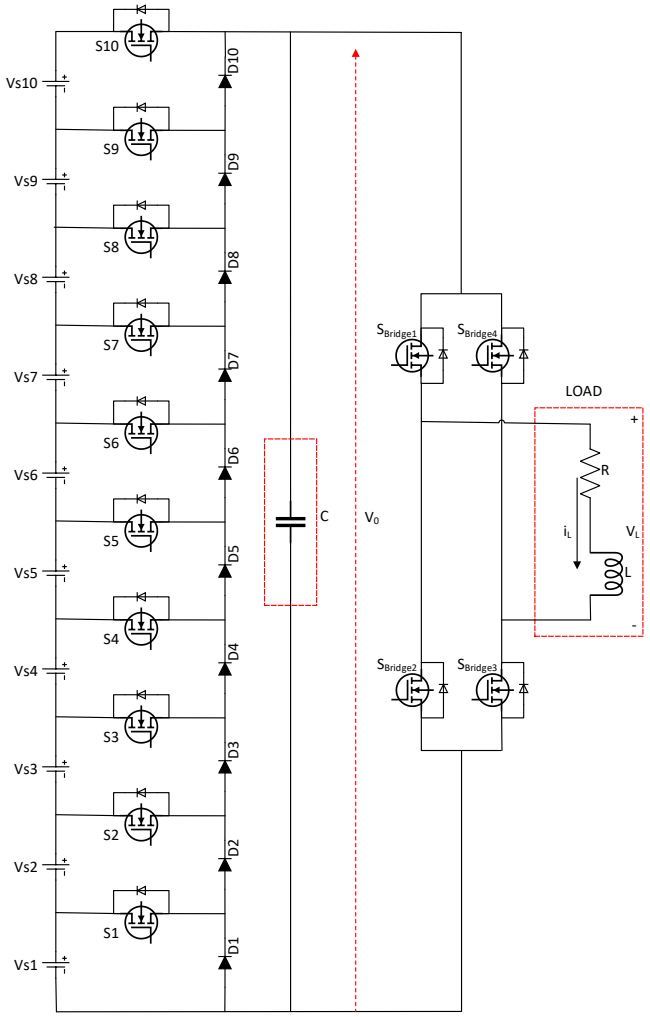


Fig. 5. The proposed new cascaded multilevel inverter topology 21 level for RL loads.

The proposed new cascaded multilevel inverter topology 21 level for RL loads in this paper shown on fig.5. By adding a capacitor to the dc bus, spike voltage due to inductive loads can be overcome. It will produce 2n+1 output voltage level, used only n+4 the number of switches needed and only 3 conducting switches at any time operation. So that the topology will be more efficient in the use of switching components and still maintain the harmonic value (THD) even though it is charged by the RL load.

3. Simulation The Proposed Cascaded Multilevel Inverter

The simulation circuit is based on the topology in fig.5. To calculated the maximum current flow in the switching device can use the equation (5) for the output power (Po) 600W, assuming an efficiency of η = 0.94% and an output voltage of Vo = 180V. Then obtained the following relationship [3]:

$$I_{switch} = \frac{\left(\frac{P_o}{\eta}\right)}{V_o} \tag{5}$$

$$= \frac{\left(\frac{600}{0{,}94}\right)}{180} = 3{,}55\ A$$

If the inverter is connected to inductive loads, voltage spikes occur due to self-induced emf (back emf) at the base of the step sine wave. The reverse current of the load, i_L is blocked by the diode used to deactivate the internal MOSFET diode that is turn on, suddenly reducing the current flowing in the inductive component of the load and the inductive component of the load will generate a high voltage spike due to the collapse of the magnetic field in a very short time. The spike voltage can be removed by using a capacitor on the dc bus.

The reactive power of the load produced by an inductive load will determined the size of the capacitor value. The value of capacitor is calculated by the following equation (6).

$$C_{(uF)} = \frac{Q_L}{2\pi f V_{L(rms)}{}^2} \times 10^6 \tag{6}$$

The size of the capacitor value (C) depends on the value of reactive power (Q_L), the frequency of the sine wave (f) and the value of the output voltage ($V_{L(rms)}$). The function of this capacitor is to compensate or minimize the reactive power generated by the induced load.

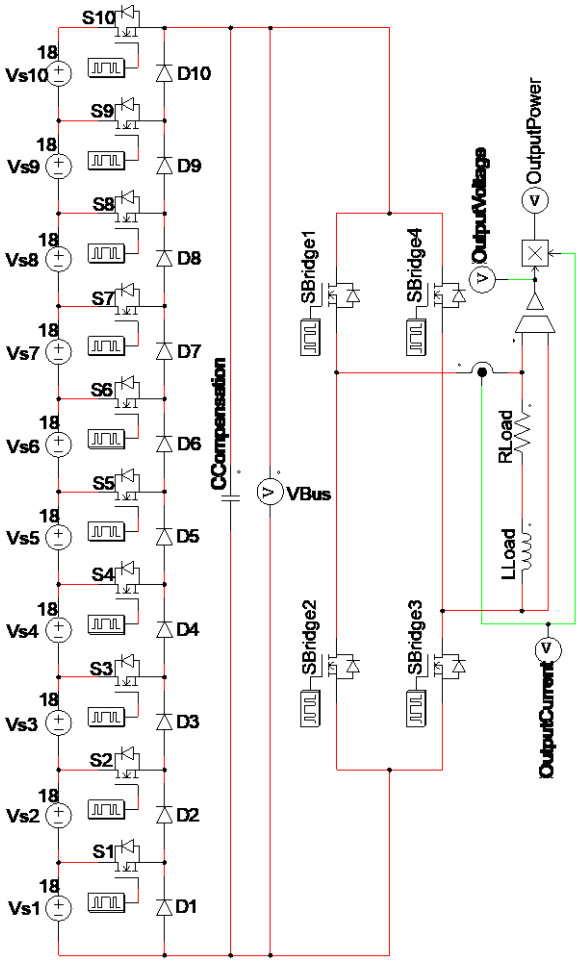


Fig. 6. Simulation circuit for the proposed new cascaded multilevel inverter topology 21 level for RL loads.

Table 1. Component Used

No	Type of Component	Quantity	
		[9]	The Proposed New Topology
1	Switch for level	22	10
2	Switch for H bridge	4	4
3	Diode	11	10
4	Resistor for simulation R loads	5	5
5	Inductor for simulation L loads	5	5
6	Capacitor	0	5

Table 2. R, L, C Value

Size of The Value	Simulation No.	Type of Topology	
		[9]	The Proposed New Topology
R (Ω)	1	12	12
	2	14	14
	3	16	16
	4	18	18
	5	20	20
L (mH)	1	78	78
	2	74	74
	3	70	70
	4	65	65
	5	59	59
C (μF)	1	-	102,14
	2	-	96,88
	3	-	90,72
	4	-	84,08
	5	-	76,64

To produce a 21-level MLI like proposed the new topology (see fig.6), it takes 10 DC voltage sources with several electronic components shown on Table 1. Five variable sizes of resistor and inductor is used as a presentation of several load values in simulation. The load variation and capacitor compensation values can be seen in Table 2. Each DC source is 18 Volt and H Bridge circuit is used to change the polarisation of the output to become sine wave.

4. Simulation Result

This inverter topology is designed for stand-alone systems with resistive (R) and inductive (L) loads. This simulation uses PSIM Professional Version 9.1.4. The output waveform of the multilevel inverter is determined by switching signal. Simulation results for output voltage waveform at the generation level (VBus) is shown in fig.7a and the output voltage and current (Voutput and Ioutput) is shown in fig.7b.

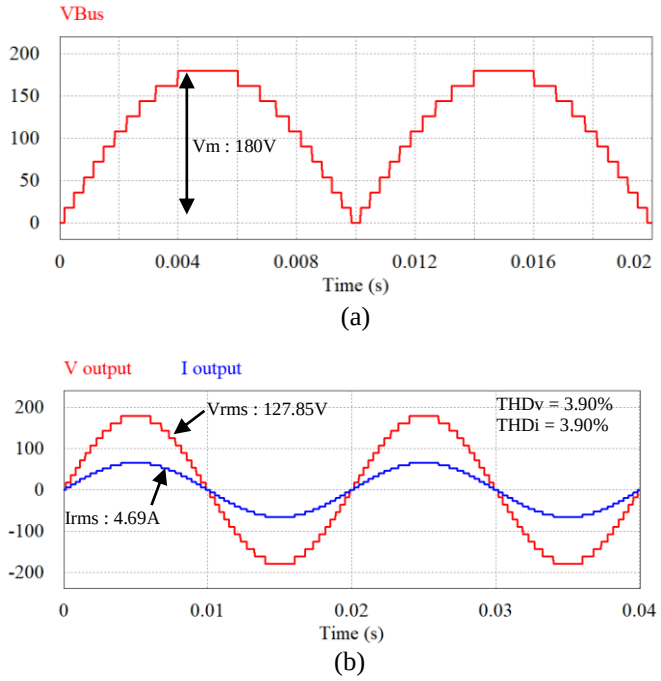


Fig. 7. Simulation output waveforms at a resistive load of 27.24Ω.
(a) Waveform at V_{Bus} (b) Waveform at V_O and I_o

The output waveform from the simulation using resistor (R=12Ω) and inductor (L=78mH) as the inductive load and with the installation of a compensation capacitor of 102.14 µf can be seen in fig.8.

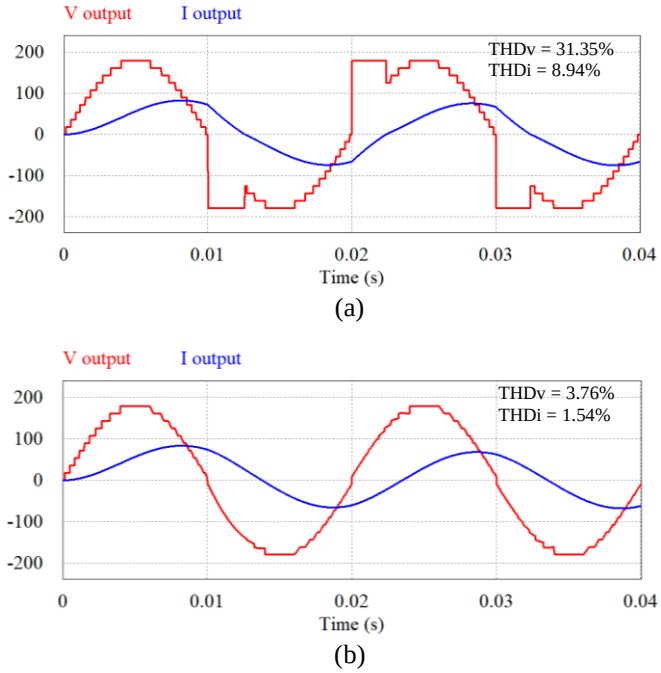


Fig. 8. Simulation output waveform at an inductive load (R=12Ω and L=78mH).
(a) The proposed new topology without capacitor. (b) The proposed new topology using a capacitor 102.14µF.

The output waveform from the simulation using resistor (R=14Ω) and inductor (L=74mH) as the inductive load and with the installation of a compensation capacitor of 96.88 µf can be seen in fig.9. The output waveform from the simulation using resistor (R=16Ω) and inductor (L=70mH) as the inductive load and with the installation of a compensation capacitor of 90.72 µf can be seen in fig.10.

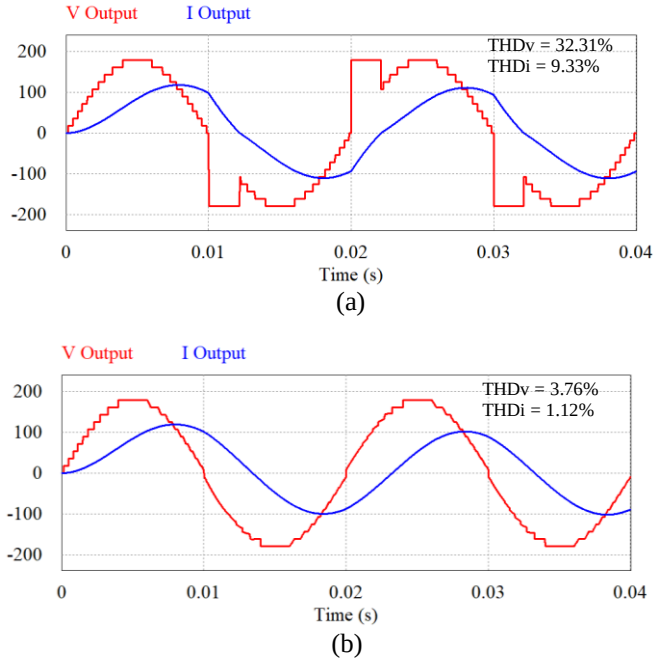


Fig. 9. Simulation output waveform at an inductive load (R=14Ω and L=74mH).
(a) The proposed new topology without capacitor. (b) The proposed new topology using a capacitor 96.88µF

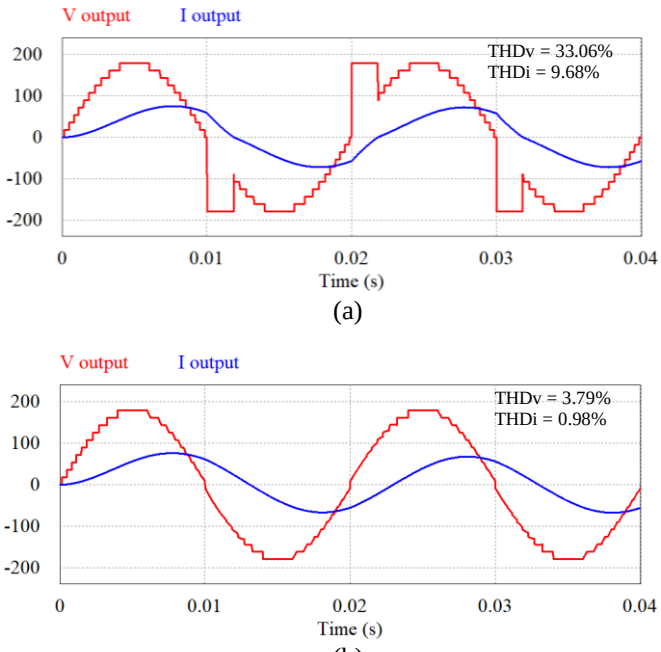


Fig. 10. Simulation output waveform at an inductive load (R=16Ω and L=70mH).
(a) The proposed new topology without capacitor. (b) The proposed new topology using a capacitor 90.72µF

The output waveform from the simulation using resistor (R=18Ω) and inductor (L=65mH) as the inductive load and with the installation of a compensation capacitor of 84.08 µf can be seen in fig.11. The output waveform from the simulation using resistor (R=20Ω) and inductor (L=59mH) as the inductive load and with the installation of a compensation capacitor of 76.64 µf can be seen in fig.12.

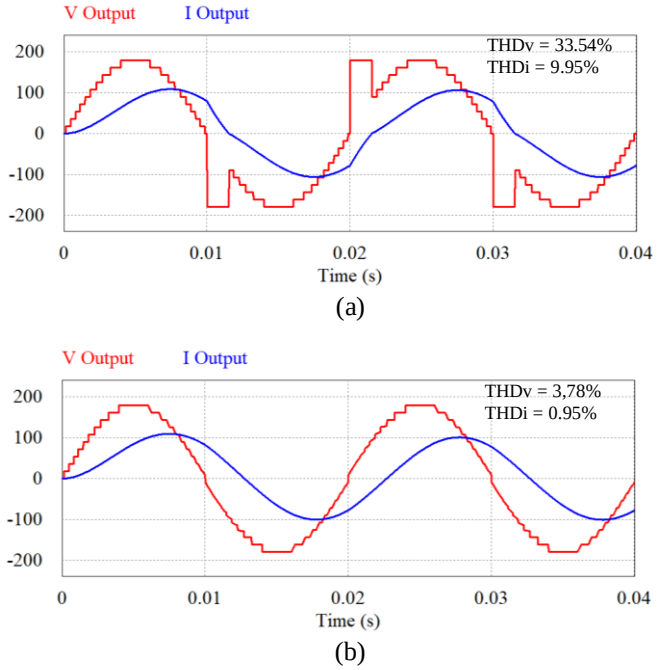


Fig. 11. Simulation output waveform at an inductive load (R=18Ω and L=65mH).
(a) The proposed new topology without capacitor. (b) The proposed new topology using a capacitor 84.08µF

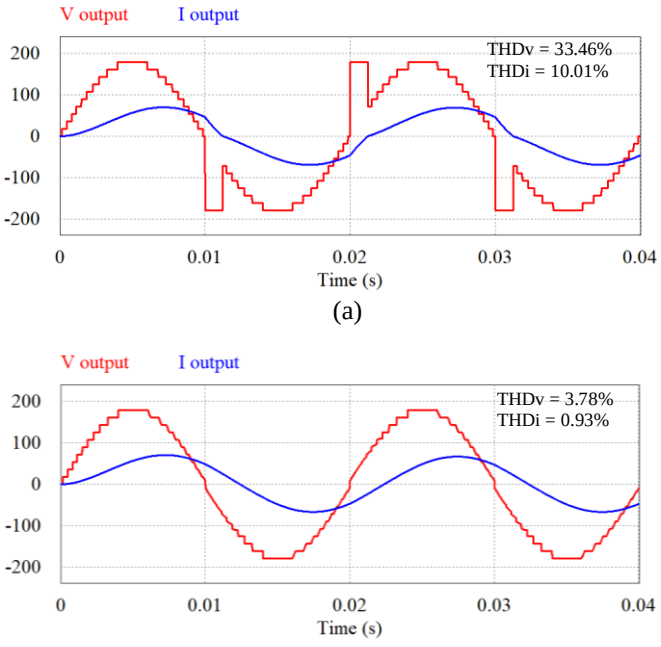


Fig. 12. Simulation output waveform at an inductive load (R=20Ω and L=59mH).

(a) The proposed new topology without capacitor. (b) The proposed new topology using a capacitor 76.64µF

Table 3. Comparison THDv and THDi

Simulation No.	Type of Topology			
	[9]		The Proposed New Topology	
	THDv (%)	THDi (%)	THDv (%)	THDi (%)
1	3.90	2.06	3.76	1.54
2	3.90	0.86	3.76	1.12
3	3.90	0.37	3.79	0.98
4	3.90	0.22	3.78	0.95
5	3.90	0.22	3.78	0.93

Table 4. Comparison of Number of Switches Needed for Different Output Voltage Levels and Number of Conducting Switches During Inverter Operations

Output Voltage Levels	Number of Switches Needed		Number of Conducting Switches During Operation	
	[9]	The Proposed New Topology	[9]	The Proposed New Topology
11	16	9	4	3
21	26	14	4	3
31	36	19	4	3
41	46	24	4	3
51	56	29	4	3

Comparison of THDv and THDi between research [9] and the proposed new topology can be seen in Table 3. Reducing the number of switches component in the proposed new topology can still produce a sine wave with a better THDv even when subjected to resistive (R) and inductive (L) loads. The THDi value was slightly higher when compared to research [9] but still far less than the maximum limit set by the IEEE STD 519 2014 standard [8].

By looking at Table 4, we can conclude that the number of switches needed for different output voltage levels and number of conducting switches during inverter operations in the proposed new topology is less when compared to research [9] so that the use of components and circuit work becomes more efficient.

The total harmonic distortion (THD) of the proposed new topology based on 5 simulations can be seen in fig.13.

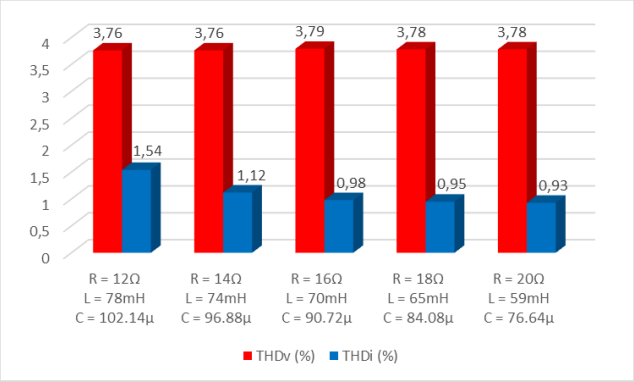


Fig. 13. Values of THDv and THDi are based on simulation results of the proposed new topology

5. Conclusion

The cascade multilevel inverter proposed in this paper obtains quite good results when compared to other topologies for certain power ranges. Based on the simulation results with varying RL loads, it was found that by installing a capacitor can overcome the reverse current and spike voltage. The size of the capacitor value is determined based on the reactive power of the load produced by an inductive load. The higher value of the induced load will make the reactive power also increase and the size of capacitor value also increase. The proposed new topology can generate 21 level with 14 switches needed and 3 conducting switches during operation.

The proposed new topology is efficient in value of THDv and THDi, number of switches needed for different output voltage levels and number of conducting switches during inverter operations.

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