Cascaded Inductively Coupled DSTATCOM for Improved PQ Performance

Praveen Kumar Yadav Kundala *, Mrutyunjaya Mangaraj **, Suresh Kumar Sudabattula***

*Department of Electrical and Electronics Engineering, Lovely Professional University, Punjab, India-144402

** Department of Electrical and Electronics Engineering, Lendi institute of engineering and technology, JNTUK, Vizianagaram, India-535005

*** School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India-144402

(praveen263@mail.com, mmangaraj.ee@gmail.com, suresh.21628@lpu.co.in)

‡ Corresponding Author; Praveen Kumar Yadav Kundala, Punjab, India-144402, Tel: 9985157790, praveen263@gmail.com

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Abstract- This study presents the comprehensive analysis of cascaded inductively coupled distributed static compensator (CIC-DSTATCOM) using icosϕ control technique for electric power distribution system (EPDS). The relevant advantages of this recommended CIC-DSTATCOM controller exhibits higher reliability, easier extension and better compensation capabilities under load perturbation. With this motivation, initially cascaded direct coupled distributed static compensator (CDC-DSTATCOM) is considered for power quality (PQ) improvement by employing icosϕ controller. The control algorithm is implemented to generate the reference current which further helps to generate the appropriate switching pulses for the DSTATCOM. Later to this, the design is extended for CIC-DSTATCOM on the same EPDS employing inductively filter converting transformer (IFCT). Supremacy of the proposed approach is shown by comparing the results among both CIC-DSTATCOM and CDC-DSTATCOM. Finally, the improved performance analysis of the proposed method is carried out for harmonics reduction 3.14%, 0.99 improved power factor (PF), load balancing, and potential regulation under load varying parameters and maintained improved PQ performance within the range of benchmark value of the IEEE-2030-7-2017 and IEC-61000-1 grid data.

Keywords CDC-DSTATCOM, CIC-DSTATCOM, VSI, icosØ control algorithm, PQ Improvement.

1. Introduction

The prime motivation of EPDS is attracted to the consumers and service provider to provide secure, reliable, quality, efficient and economical source of electrical energy. Hence, the EPDS is required to be properly planned, designed and safely operated. Generally, EPDS is subjected to more number of faults/disturbances during the operation [1]-[2]. Increase in electrical power demands, lack of long-term planning, open access to consumers, minimum security, nonlinear loads, unplanned load switching are the reasons for degrading quality of supply [3]-[4].

Hence, the power system operating professionals need new techniques for improving the PQ performance [5]-[6]. With this motivation for improving the PQ performance in the EPDS, the DSTATCOM is the important choice for current related PQ issues [7]-[8]. Even though, DSTATCOM is playing an important role in the EPDS, still, on the other side of the coin, diversification of the DSTATCOM is a growing role for the modern EPDS. Hence, the challenging task is to provide flexibility and sustainability for all above scenarios [9]-[10]. Pertinent selection of voltage source inverter (VSI), extension of VSI, design of control algorithm, IFCT design, impedance matching are the major research areas for the improvement of the PQ [11]-[12]. From last three decades, most of the researchers and several R&D organizations focused on different custom power devices (CPD) to neutralize the PQ based problems [13]-[14]. All the CPDs perform flexible, reliable and quick reaction to inject reactive power at point of common coupling (PCC) of system [15]-[16]. In CDC-DSTATCOM the PCC experiences more stress because of direct contact between supply, load & DSTATCOM. Hence, more chances to flow of short circuit currents, poor protection, and thermal losses etc [17]-[18]. Also it cause to increase harmonic loss, noise and mechanical imbalance. Hence, the new step has to be taken to overcome the demerits of CDC-DSTATCOM. Hence, the research direction is motivated to step forward for the remedial solution by using IFCT. The purpose of IFCT to introduce in this study, to damp out the harmonics resonance in between source and filtering side, which further does not allow the harmonics to flow in to the source side. So that, PQ improvement with stable operation will be acheived.

First of all, this paper is dealt with the design of CDC-DSTATCOM for EPDS [19]-[20]. Later to this, the IFCT is introduced with CDC-DSTATCOM to behave as an inductive medium between source and load [21]-[22]. In addition to this, another set of similar kind of VSI is connected in cascade through the suitable value of inductor in every phase to justify the recommended topology for the EPDS. It bears number of merits such as less switching stress, improved balance voltage at PCC, increasing the compensation capability, and other different combinations are possible [23]-[24]. In view of the design aspect of the DSTATCOM, two level voltage source converters are considered for three phase three wire (3P3W) EPDS [25]. This three leg VSI topology is widely put forward due to its own popularity in the literature survey. The projected topology affords flexibility for future improvement for connecting additional converters and loads [26]-[27].

For healthier operation of DSTATCOM, the filtering mechanism is performed by following the generalized mathematical approach using $icos\emptyset$ algorithm using MATLAB/ Simulink. The following observations are inferenced from the proposed CIC-DSTATCOM scheme in accordance with the standard set by IEEE-2030-7-2017 & IEC- 61000-1 grid data.

- Good convergence performance is obtained.
- The main features of this algorithm are enhanced tracking, adaptive, and compensatory capacities.
- The anticipated structure supports for accomplishing the numerous PQ issues like harmonics reduction, healthier potential regulation, PF rectification, load equalizing and reduction in DC link voltage etc.
- It also provides the flexible protection against of harmonics over current.
- It is capable to restructure the additional parameters for improved version of algorithm.

The above section summarizes the literature view of the case studies. The detailed structure of network structure & modelling of both CDC-DSTATCOM & CIC-DSTATCOM is placed in section-2. Section-3 carries modelling and design of IFCT. System topology followed by $icos\emptyset$ algorithm using MATLAB/Simulink platform presented in section-4. The subsequent comparative simulation results are situated section-5. Finally,the effectiveness of the system is summarized in section-6.

2. Modeling of the Proposed Cic-Dstatcom

The arrangement of the 3P3W EPDS with CDC-DSTATCOM and CIC-DSTATCOM are shown in Fig.1 & 2 respectively. The CDC-DSTATCOM which consists of balanced 3-phase supply, DSTATCOM, non-linear load (uncontrolled rectifier), whereas the CIC-DSTATCOM which consists of a balanced 3-phase supply, converter transformer DSTATCOM, three-phase non-linear load. The VSI based DSTATCOM associated at PCC of EPDS is exposed in Fig.3. An adapted technology of self supported capacitor based CDC-DSTATCOM & CIC-DSTATCOM are utilized as like compensator to lessen the PQ matters. The switching signals for IGBTs of the both compensators are created by icosϕ control technique. This study's goal is to employ this control algorithm in order to choose a reliable method.

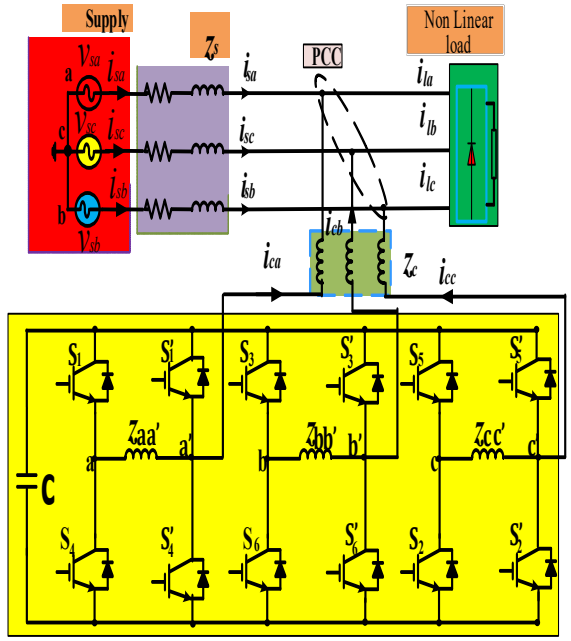

Fig. 1. EPDS with CDC- DSTATCOM.

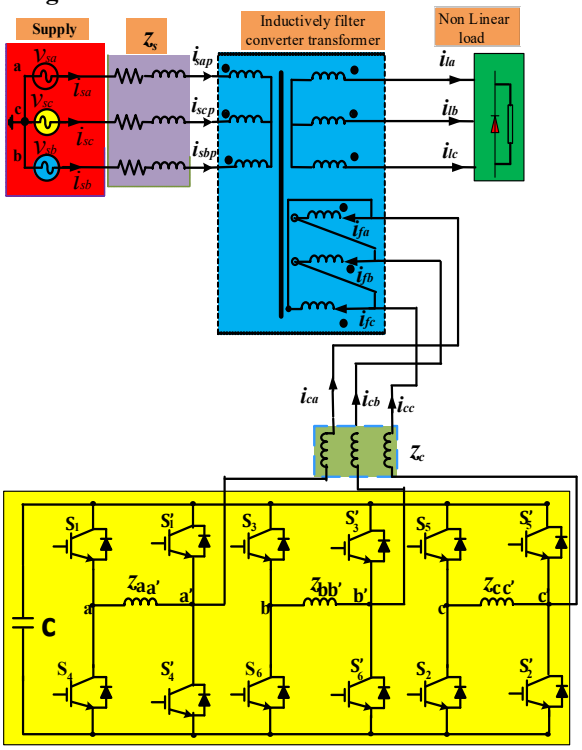

Fig. 2. EPDS with CIC- DSTATCOM

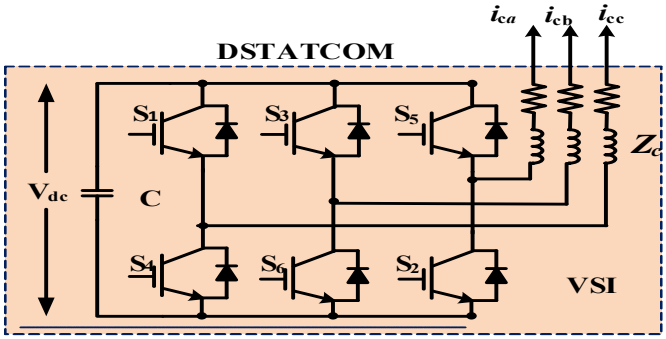

Fig. 3. Two-level self-supported capacitor supported VSI based DSTATCOM

The proposed cascaded module includes 12 semiconductor switches and placed together with an appropriate connection with inductor linking which is shown in fig.2. as shown in fig $S_1 – S_6$ switches are ---------- whereas $S_1^1 – S_6^1$ are choosen for other limb to ----- the voltage balancing and reducing switching stress, consequently each limb of full bridge inverter is achieved bipolar --- in this inverter, inductors (Z_{AA}^1, Z_{bb}^1, Z_{cc}^1) are used to enable the bidirectional current flow and block positive off state voltage.

2.1. Innovations of Anticipated Method

There are numerous innovations of the anticipated topology:

- Drop in structure down time cost: The overall load output current is dependent on converter transformer and VSC interfacing impedance, which reduces the unsuccessful rate of IGBT. So, dropping in structure down time-cost will improve the dependability of the EPDS.
- Drop in VSC rating: The current fed by VSC is lessened due to converter transformer and VSC interfacing impedance therefore the rating of VSC is reduced.
- Flexible operation of inverter: AS VSC is connected through the converter transformer which permits to easy maintenance which additional improves the flexibility of the EPDS.
- Increase in system efficiency: The system efficiency is increased due to matching impedance in between converter transformer and VSC interfacing impedance.
- Drop in total harmonic distortion (THD) of the input current: The THD of input supply & output load current are 3.14% & 27.90% correspondingly taken from CIC-DSTATCOM. Where, the THD of input supply & output load current are 4.05% & 27.90% correspondingly taken from CDC-DSTATCOM.

3. Modelling and Design of Inductive Transformer

The three-phase harmonic equivalent circuit of the specified CIC-DSTATCOM is structured in Fig-2, from this we can get clear idea about connection structure of IFCT at PCC. Both voltages and currents have their fundamental and harmonic components. The proposed CIC-DSTATCOM configures IFCT, DSTATCOM consisting VSI & non-linear load. The CDC-DSTATCOM & non-linear load both are coupled to the IFCT's three winding. The star-wired primary winding (PW), the star-wired secondary winding (SW), and the delta-wired third winding filtered winding (FW) is linked with CDC-DSTATCOM. The purpose of the specialised IFCT winding is to achieve a potential equilibrium among the grid, the load, and the DSTATCOM. That is to say the harmonics are inaccessible from the PW. The complete mathematical pattern of IFCT & filtering mechanism is analysed in the next subsections.

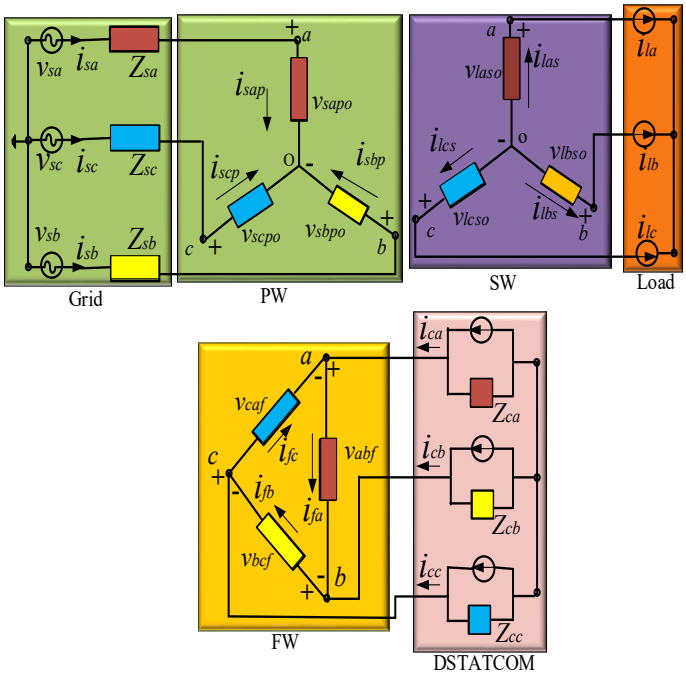

Fig.4. Equivalent circuit of proposed DSTATCOM

The voltage balance equation of PW, SW and FW can be expressed as,

$$\begin{cases} N_1 i_{sap} + N_2 i_{las} + N_3 i_{caf} = 0 \\ N_1 i_{sbp} + N_2 i_{lbs} + N_3 i_{cbf} = 0 \\ N_1 i_{scp} + N_2 i_{lcs} + N_3 i_{ccf} = 0 \end{cases} \quad (1)$$

According to Kirchhoff's current law (KCL), the current equations in the primary side of the IFCT are written as

$$\begin{cases} i_{sap} = (v_{sa} - v_{sapo})/Z_{sa} \\ i_{sbp} = (v_{sb} - v_{sbpo})/Z_{sb} \\ i_{scp} = (v_{sc} - v_{scpo})/Z_{sc} \end{cases} \quad (2)$$

According to KCL, the current equations in the secondary side of the IFCT (load side) are written as

$$\begin{cases} i_{la} = i_{las} + i_{caf} \\ i_{lb} = i_{lbs} + i_{cbf} \\ i_{lc} = i_{lcs} + i_{cbf} \end{cases} \quad (3)$$

The current balance equations are shown below:

$$\begin{cases} \mathrm{i_{sap}} + i_{sbp} + i_{scp} = 0 \\ \mathrm{i_{las}} + i_{lbs} + i_{lcs} = 0 \\ \mathrm{i_{caf}} + i_{cbf} + i_{ccf} = 0 \end{cases} \quad (4)$$

The total compensating current equations at filter side are written as

$$\begin{cases} \mathrm{i_{caf}} = i_{ca} + i_{fa} \\ \mathrm{i_{cbf}} = i_{cb} + i_{fb} \\ \mathrm{i_{ccf}} = i_{cc} + i_{fc} \end{cases} \quad (5)$$

4. Icosϕ Control Algorithm

The control assembly of the system is presented in Fig.4. Owing to its rapid & strong dynamic reaction to both stable-state & transient response, the icosϕ controller is chosen to provide the gate signals for the inverter's switches. The inside control signal of icosϕ control scheme is shown in Fig. 6. The gate signals used to operate the DSTATCOM are created using a four-stage process.

(i) In order to calculate the most basic quantity of the III-phase output load current, Fourier blocks are used.

(ii) Active and reactive load output current are generated via the same control method.

(iii) Reference supply currents are generated using the active and reactive components of the output currents in accordance with the algorithm.

(iv) Each switching signal is produced by totaling the active & reactive components of the output current that are provided to the hysteresis current controller (HCC).

Here, i_{lap} denotes the active power element of fundamental output load current is expressed as

$$\begin{bmatrix} i_{lap} \\ i_{lbp} \\ i_{lcp} \end{bmatrix} = \begin{bmatrix} Re(i_{la}) \\ Re(i_{lb}) \\ Re(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}cos\phi_{la} \\ i_{lb}cos\phi_{lb} \\ i_{lc}cos\phi_{lc} \end{bmatrix} \quad (6)$$

The weighted mean worth of the real active power element w_p

$$w_p = \left(\frac{i_{la}cos\phi_{la}+i_{lb}cos\phi_{lb}+i_{lc}cos\phi_{lc}}{3}\right) \quad (7)$$

In the similar way we can express the reactive power component.

$$\begin{bmatrix} i_{laq} \\ i_{lbq} \\ i_{lcq} \end{bmatrix} = \begin{bmatrix} Im(i_{la}) \\ Im(i_{lb}) \\ Im(i_{lc}) \end{bmatrix} = \begin{bmatrix} i_{la}sin\phi_{la} \\ i_{lb}sin\phi_{lb} \\ i_{lc}sin\phi_{lc} \end{bmatrix} \quad (8)$$

The weighted mean worth of the reactive power component w_q

$$w_q = \left(\frac{i_{la}sin\phi_{la}+i_{lb}sin\phi_{lb}+i_{lc}sin\phi_{lc}}{3}\right) \quad (9)$$

The mean worth of active & reactive weighted modules is 'w_p', 'w_q'respectively. The'w_p', 'w_q' are the clustered mass & there is assurance to give an adjusted worth. The LPF, as depicted in Fig.5, is proposed as a means of overcoming these limitations. With LPF applied, these sonic parameters dampen the greater-order harmonics. Thus, the tuned weight active element (w_{spt}) & reactive element (w_{sqt}) of output current are reached. At last, the advised control procedure is aimed to get a filtered and adjusted mass. In addition, the modified weight is less susceptible to noise and, as a result, becomes steady and adaptable to any network disturbance, which assist to vaccinate the correct compensator current at PCC. The accumulation of PI controller output & the weighted mean worth of the real active power element w_p grants the overall active elements of the reference supply input current.

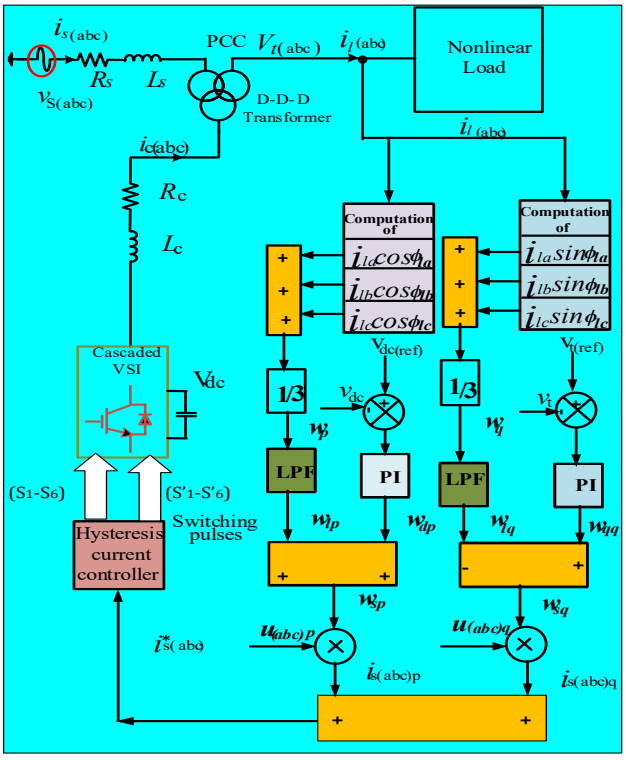

Fig. 5. Switching signals generation for CIC-DSTATCOM

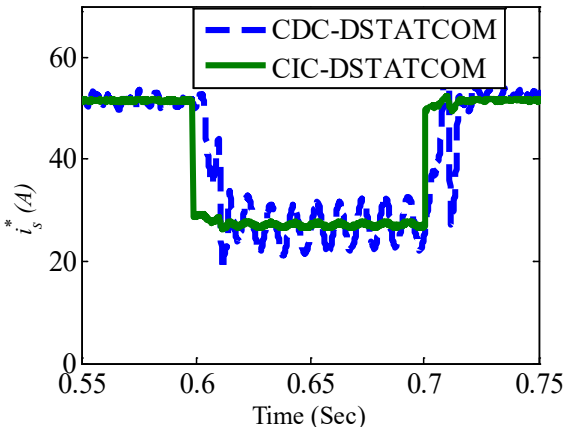

Fig. 6. Inner control signal of the control algorithm

The dc potential error (v_{de}) can measured by subtracting the sensed dc potential (v_{dc}) from reference dc potential ($v_{dc(ref)}$) and it is fed with Proportional-Integral (PI) controller to hold constant dc bus potential.

The controller's output can be outright as

$$w_{dp} = k_{pdp} v_{de} + k_{idp} \int v_{de} dt \quad (10)$$

$$w_{spt} = w_{dp} + w_{lp} \quad (11)$$

In similar manner, the overall reactive components can be outright as

$$w_{sqt} = w_{qq} - w_{lq} \quad (12)$$

A low pass filter which cut of rate is 20.1 Hz utilized for filtartion of active & reactive weighting factor of load output current.

Instantneous value of active supply currents i_{sp}, can be figured as

$$\begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} = w_{spt} \begin{bmatrix} u_{ap} \\ u_{bp} \\ u_{cp} \end{bmatrix} \quad (13)$$

Instantneous worth of the reactive supply currents i_{sq}, can be figured as

$$\begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} = w_{sqt} \begin{bmatrix} u_{aq} \\ u_{bq} \\ u_{cq} \end{bmatrix} \quad (14)$$

The refernce supply currents are illustrated as

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \begin{bmatrix} i_{sap} \\ i_{sbp} \\ i_{scp} \end{bmatrix} + \begin{bmatrix} i_{saq} \\ i_{sbq} \\ i_{scq} \end{bmatrix} \quad (15)$$

Together the actual supply currents (i_{sa}, i_{sb}, i_{sc}) and the reference supply currents ($i_{sa}^*, i_{sb}^*, i_{sc}^*$) of the respective phases are compared, next, the Hysteresis current controller (HCC) receives error signals based on the current flow. It operates as follows:

(i) when $i_{sa} < i_{sa}^*$, s_1 ON & s_4 is OFF
(ii) when $i_{sa} > i_{sa}^*$, s_1 OFF & s_4 ON

Their outputs are utilized to breed the switching signal of both CDC-DSTATCOM & CIC-DSTACOM.

5. Simulation Results and Discussion

The performance of EPDS with topologies are demonstrated using MATLAB/Simulink studies. Identical operating conditions and system parameters are considered to perform computer simulations. The suggested $icos\emptyset$ mechanism is implemented for reference current generation for appropriate switching pulses to the both varieties of topologies. The system parameters are listed in Table 5. Both the balanced and unbalanced performance of CIC-DSTATCOM and CDC-DSTATCOM based EPDS are analyzed here in the below sub-sections.

5.1. Simulation results of CDC-DSTATCOM

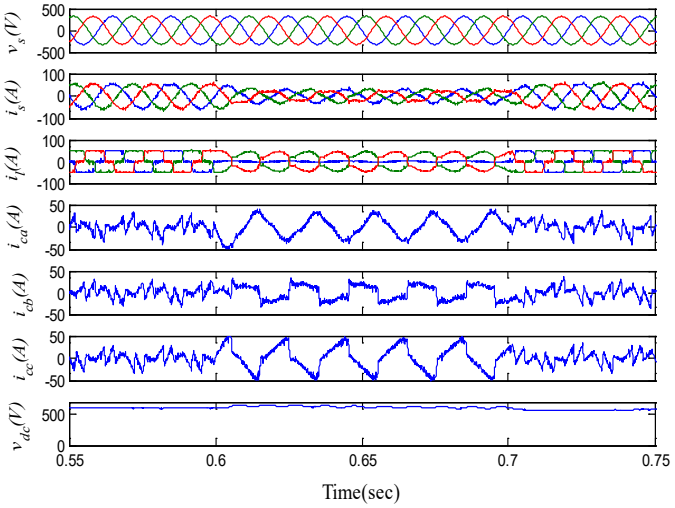

Fig. 7. a Simulation wave shape of (top to down) III- phase input potential, supply current, output load current, compensating current & DC- link potential with CDC-DSTATCOM.

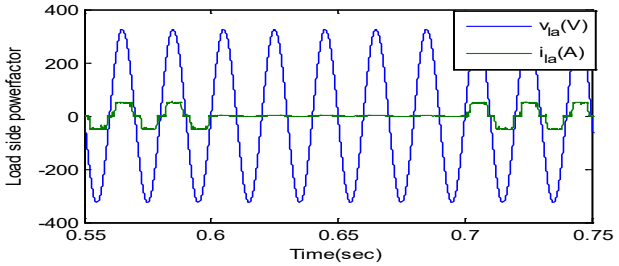

Fig.7. b Source side powerfactor with CDC- DSTATCOM

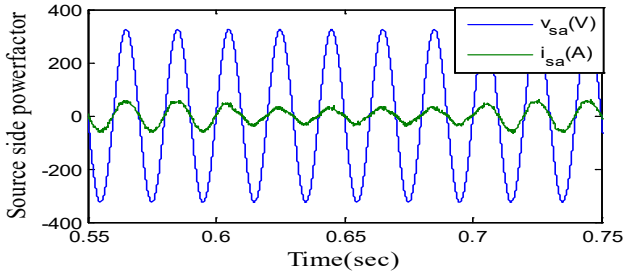

Fig. 7. c Load side powerfactor with CDC-DSTATCOM

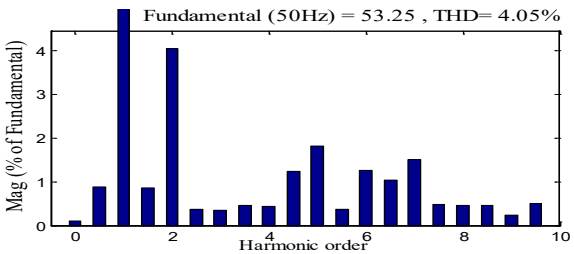

Fig.7. d Source current THD with CDC- DSTATCOM

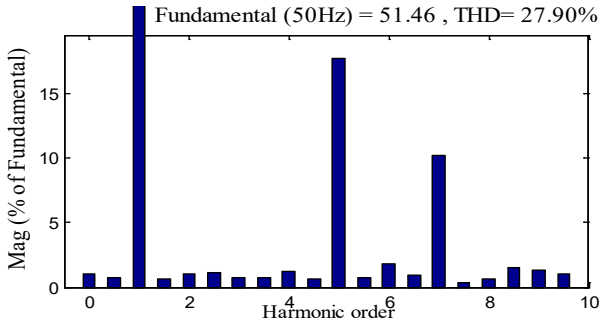

Fig. 7. e Load current THD with CDC- DSTATCOM.

The simulation study is analysed during 0.55 Sec to 0.75 Sec to maintain the uniformity. But unbalanced performance is chosen during a step drop in a-phase loading in between 0.6 Sec to 0.7 Sec. In the Fig. 7 b, the significant improvement of power factor (p.f) at source side is achieved 0.94 under this situation, whereas, Fig. 7 c shows the low power factor at load side. Figure 7d shows a 4.05% THD in the source current, while Figure 7e shows a 27.90% THD in the load current at the output. This indicates the significant supply current harmonics discount based on IEEE-2030-7-2017 & IEC- 61000-1 standard. The voltage regulation is maintained due to 535V desired and uniform DC link potential. Finally, 320V is keep up at PCC for satisfying the voltage balancing.

5.2. Simulation outcomes of CIC- DSTATCOM

The performance of the CIC- DSTATCOM based EPDS under both balanced and unbalanced loading is depicted in Fig.8 a. In this figure, several subplots such as supply potential, supply current, output load current, compensator current & DC-link potential are indicated down from the top. The simulation study was analysed during 0.55 Sec to 0.75 Sec to maintain the uniformity. But unbalanced performances are chosen during a step drop in a-phase loading in between 0.6 Sec to 0.7 Sec. In the Fig. 8 b, the significant improvement of power factor (p.f) at source side is achieved 0.99 under this situation, whereas, Fig. 8 c shows the low pf at load side. The source current THD% is 3.14 which depicted in Fig.8 d, whereas the load current THD% is 27.90 which is shown in Fig.8 e.

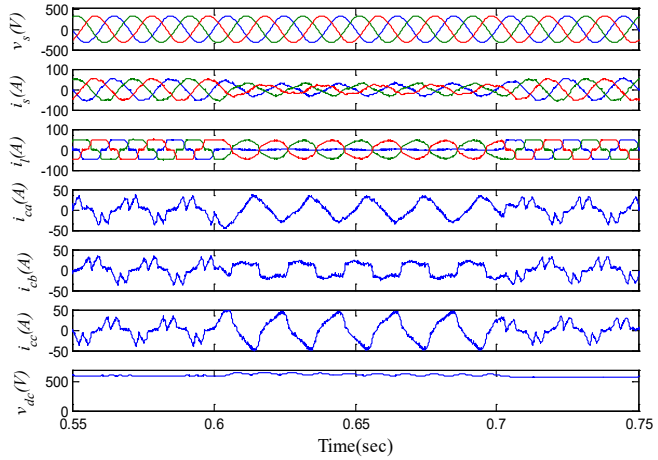

Fig. 8. a Simulated wave shape (top to down) III- phase input potential, supply current, output load current, compensating current, DC-link potential with CIC-DSTATCOM

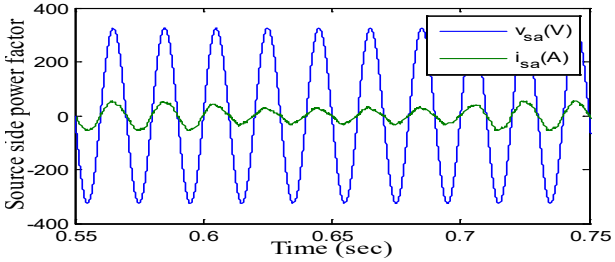

Fig. 8. b Source side powerfactor with CIC-DSTATCOM

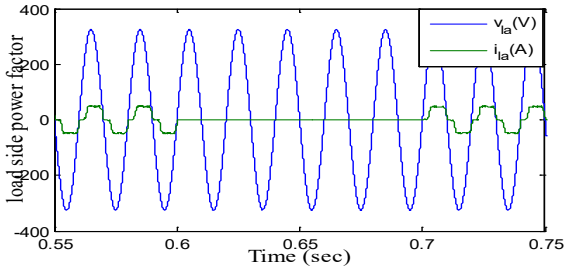

Fig. 8. c Load side powerfactor with CIC-DSTATCOM

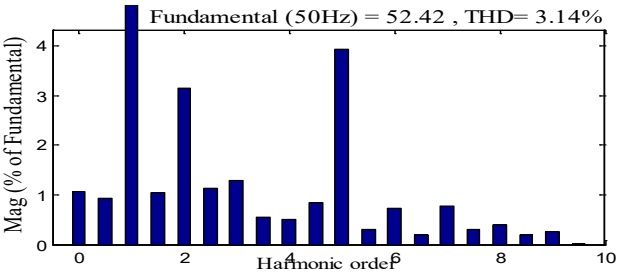

Fig. 8. d Source current THD with CIC-DSTATCOM

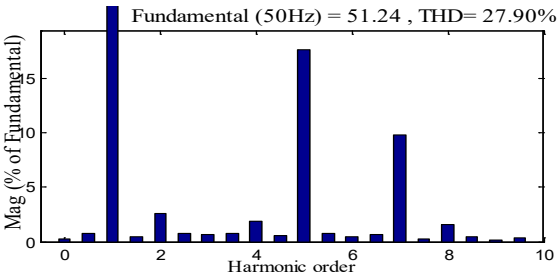

Fig. 8. e Load current THD with CIC-DSTATCOM

Table.1. Performance parameter of CDC-DSTATCOM and CIC-DSTATCOM

Performance parameter	DSTATCOM at PCC		
	IC-DSTATCOM[5]	CDC-DSTATCOM	CIC-DSTATCOM
i_s(A), %THD	55.6, 4.14	53.25, 4.05	52.42, 3.14
v_s (V), %THD	330, 2.15	321.4, 2.23	321, 1.42

i_l (A), %THD	51.34, 27.90	51.46, 27.90	51.24, 27.90
Power Factor	0.97	0.94	0.99

Table.2. Basic rating parameters of the IFCT

	Grid side	Load side	Filtering side
Wiring scheme	Wye	Wye	Delta
Nominal power and	10kV, 50 Hz	10kV, 50 Hz	10kV, 50 Hz
Voltage (ph-ph), R, and	230V, 0.002 (pu), 0.08	230V, 0.002 (pu), 0.08 (pu)	230V, 0.002
Magnetic resistance	500 Ω	500 Ω	500 Ω
Magnetic inductance	500 Ω	500 Ω	500 Ω

Table.3. Measured active and reactive power of IFCT

Grid side	Active power reactive power	26 kW 1.388 kVAR
Load side	Active power reactive power	15 kW 1.388 kVAR
Filtering side	Active power reactive power	24 kW 570 VAR

The performance analysis of the both CDC-DSTATCOM and CIC-DSTATCOM are indicated in Table-1. The proposed CIC-DSTATCOM diminished a greatly polluted supply current harmonics from EPDS as compared to other.

5.3.1. Analysis of kVA rating

The Volt ampere (kVA) rating can be obtained as VA rating=$\sqrt{3}*\frac{I_f v_{dc}}{\sqrt{2}}$

Where v_{dc} is the DC link potential of DSI and I_f is the inverter current

kVA rating of CDC-DSTATCOM = $\sqrt{3}*\frac{12.5(535)}{\sqrt{2}}=$ 8.19 kVA

kVA rating of CIC-DSTATCOM = $\sqrt{3}*\frac{10.5(535)}{\sqrt{2}}=$ 6.88kVA

5.3.2. Calculation of Derating Factor (DF)

DF=1-efficiency Efficiency = $\frac{\text{output power}}{\text{input power}}*100$

kVA rating of CDC-DSTATCOM = 5.79 kVA, power factor cosϕ = 0.97

kW output of the CDC-DSTATCOM = kVA* cosϕ = 5.794*0.97 = 5.62 kW

Power losses of CDC-DSTATCOM = $3I_f^2 * R_c$

I_f is the inverter current= 12.5 A, R_c= 0.25 Ω

$3I_f^2 * R_c = 3*12.5^2 * 0.25 = 117.18$ W

Power input = output power + losses = 5620+117.18 = 5737.18 W = 5.737 kW

Efficiency of CDC-DSTATCOM = $\frac{5.62}{5.737}*100 = 97.65\%$

DF of CDC-DSTATCOM = 1- efficiency = 1- 0.97 = 0.03

The power efficiency of CIC-DSTATCOM can be calculated by the following

kVA rating of CIC-DSTATCOM = 4.867 kVA, power factor cosϕ = 0.99

kW output of the CDC-DSTATCOM = kVA* cosϕ = 4.867*0.99 = 4.81 kW

I_f is the inverter current= 10.5 A, R_c= 0.25 Ω

$3I_f^2 * R_c = 3*10.5^2 * 0.25 = 82.68$ W

Power input = output power + losses = 4810 + 82.68 = 4892.68 W = 4.89 kW

Efficiency of CIC-DSTATCOM = $\frac{4.81}{4.89}*100 = 98.36\%$

DF of CIC-DSTATCOM = 1- efficiency = 1- 0.983 = 0.017

5.3.3. Harmonic Compensation Ratio (HCR)

The HCR of CDC-DSTATCOM is calculated as follows

HCR= $\frac{\text{THD\% after compensation}}{\text{THD\% before compensation}} = \frac{4.05}{27.90} = 0.145$

Similarly, the HCR of CIC-DSTATCOM is given as

HCR= $\frac{THD\%\ after\ compensation}{\text{THD\% before compensation}} = \frac{3.14}{27.90} = 0.112$

5.3.4. Distortion Index (DIN)

Taylor series expansion for small ranks of harmonics is below

DIN = THD (1- $\frac{1}{2}$(THD))

DIN for CDC-DSTATCOM = 4.05(1- $\frac{1}{2}$ 4.05) = -4.15

DIN for CIC-DSTATCOM = 3.14 (1- $\frac{1}{2}$ 3.14) = -1.78

5.3.5. Form Factor (FF)

The form factor is defined as FF = $\frac{I_{rms}}{I_{avg}}$

FF for CDC-DSTATCOM =

I_{rms}= 39.21 A $I_{rms} = \frac{\pi}{2\sqrt{2}} I_{avg}$ I_{avg}=35.30A

FF= $\frac{39.21}{35.30}$= 1.11

FF for CIC-DSTATCOM =

I_{rms}= 37.9 A I_{avg}=34.12A

FF= $\frac{37.9}{34.12}$= 1.11

5.3.6. *Ripple Factor (RF)*

RF is measure of the ripple content of the waveform

RF= $\frac{I_{AC}}{I_{DC}}$

RF= $\frac{\sqrt{(I_{rms})^2-(I_{DC})^2}}{I_{DC}}$= $\sqrt{(FF^2)-1}$

RF for CDC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48

RF for CIC-DSTATCOM = $\sqrt{(FF^2)-1}$= $\sqrt{(1.11^2)-1}$ = 0.48

5.3.7. *Harmonic Factor (HF)*

The HF of the h_{th} harmonic, $HF_h = \frac{I_{rms}^{(h)}}{I_{rms}^{(1)}}$

HF for CDC-DSTATCOM = $\frac{39.21}{53.25} = 0.736$

HF for CIC-DSTATCOM=$\frac{37.9}{52.42}$ = 0.72

5.3.8. *C-Message Weights*

The C-Message weighted index is very similar to the TIF except that the weights c_i are used in place of w_i

C= $\frac{\sqrt{\sum_{i=1}^{\infty}(C_i I^{(i)})^2}}{\sqrt{\sum_{i=1}^{\infty}(I^{(i)})^2}}$ C= $\frac{\sqrt{\sum_{i=1}^{\infty}(C_i I^{(i)})^2}}{I_{rms}}$

C-Message weights for CDC-DSTATCOM = $\frac{39.21^2}{53.25^2}$ = 0.5

C-Message weights for CIC-DSTATCOM = $\frac{37.9^2}{52.42^2}$ = 0.5

Table.4. Comparative study on kVA rating, DF, HCR, DIN, FF, RF, HF and C-Message weight of CDC-DSTATCOM and CIC-DSTATCOM

Sl. No.	Types of configurations	Analysis of KVA rating	DF	HCR	DIN	FF	RF	HF	C-message weight
1	**CDC-DSTATCOM**	8.19	0.03	0.145	-4.15	1.11	0.48	0.736	0.5
2	**CIC-DSTATCOM**	6.88	0.017	0.112	-1.78	1.11	0.48	0.72	0.5

Table.5. Simulation configuration parameters

Sign	Description	Worth
v_s	3- phase supply potential	230V/phase
f_s	Frequency	50Hz
R_s	input resistance	0.5Ω
L_s	input inductance	2mH
K_{pr}	AC P- controller	0.21
K_{ir}	AC I controller	1.10
v_{dc}	DC link potential	600V
C_{dc}	Capacitor	2000μF
K_{pa}	DC P-controller	0.01
K_{ia}	DC I- controller	0.05
R_c	VSC resistance	0.25Ω
L_c	VSC inductance	1.5mH

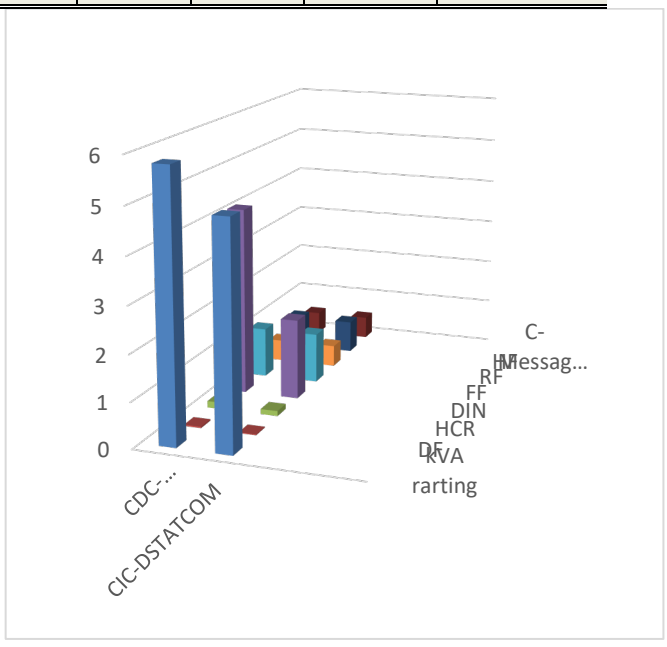

Fig. 9. Bar chart for the indexed parameters

Finally, the bar chart for the indexed parameters is presented in Fig. 9, It is observed that the proposed study

reveals the applicability and suitability for the PQ improvement.

6. Conclusion

In this research work, two different types of CIC-DSTATCOM and CDC-DSTATCOM topologies are presented. The key features of the proposed topology is highlighted as follows:

- The Performance observed from the proposed topology is suitable from the application prospective of industrial and power utility sectors.
- Inclusion of IFCT caused to improve the output AC voltage at inverter side.
- The advantages like low voltage stress, less switching loss and higher efficiency are observed.

Apart from these above mentioned merits, load balancing, source current harmonics elimination (% THD at source side 3.14), voltage regulation, pf improved to 0.99 are obtained based on benchmark worth of IEEE-2030-7-2017 & IEC- 61000-1 grid data. The simulation analysis is carried out for the selection of topology among two approaches under unavoidable circumstances of loading. With these benefits, a thorough real time analysis will be the key features for the future work.

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