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A Novel Multi-Step Model Predictive Control Design for Three-phase T-Type Inverter in Grid-Connected Mode

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Abstract- In this paper, a novel multi-step model predictive control (MPC) is proposed for the control design of a three-phase T-Type inverter in grid-connected mode. With a modification in the cost function, multiple objective optimization solutions can be achieved, i.e., switching sequence optimization, capacitor voltage balance, and common-mode voltage (CMV) minimization. In addition, the computational burden, which is always an issue of the MPC, is reduced by utilizing the sphere decoding algorithm (SDA). To verify the effectiveness of the proposed method, as well as the advantages of the multi-step MPC in comparison with its single-step counterpart, numerical simulations using Matlab/Simulink, are conducted.

Keywords Multi-step model predictive control, T-type inverter, SDA

1. Introduction

Nowadays, multi-level inverters (MLIs) have become more and more popular as a solution to replace the conventional voltage source inverters (VSIs) thanks to its outstanding advantages: low harmonic distortion, low switching frequency, low voltage drop on switches [1]. The most common used MLI structure in the literature as well as in practice are: neutral point clamped (NPC) [2], flying capacitor (FC)[3], and Cascaded H-Bridge (CHB) [4]. As the most advanced structure of the NPC family, T-Type topology has some noticeable merits. Since only one DC bus is required, the unbalance voltages between power cells, which is the major problem of the CHB converters, is removed. Besides, the number of components, i.e., diodes, capacitors, and semiconductor switches are also less than those are required in other MLI topologies [5-7].

With the above-mentioned merits, studies on the application of the T-Type converter in grid-connected mode have become attractive to researchers. It is well-known that the current controller plays a key role and decide the performance of the grid-connected converters. Hence, most researches focus on improving the performance of the inductor current-loop. Initially, linear controllers are widely used because of their simplicity. However, slow dynamic response, coupling between control channels as well as the difficulty in adjusting the controller parameters are main issues of this method. To improve the dynamic response, the direct power control (DPC) has been proposed in which linear controllers and space vector modulation (SVM) are replaced by simple hysteresis controllers and an optimum switching-state selector. This approach results in much less computational time and a much faster transient response. However, fluctuation in active and reactive power is a problem of the DPC. Other advanced control methods have also been proposed to enhance the performance of the inductor current controller, e.g., DPC with SVM, fuzzy control, sliding control, predictive control [8]. However, the T-Type converter needs a comprehensive control solution where multiple objectives must be considered. This is due to the fact that the T-Type topology itself also has several drawbacks.

First, the common-mode voltage (CMV), which is generated by high switching frequency and dead-time [9], may cause over-voltage, electromagnetic interference (EMI) noise [11], and leakage current in renewable energy systems [10]. As a result, the reliability of the grid-connected system is degraded. Various strategies to reduce the CMV based on adjusting the pulse width modulation (PWM) have been proposed [12,13]. However, the complexity of the fixed PWM

modulator decline the ability to track the desired inductor current.

The second issue of the T-Type topology is the voltage balance between two capacitors of the DC bus [14]. The voltage imbalance has negative impacts on the output voltage quality as well as the THD of output current. Conventional strategies, where PWM technique and simple linear controllers, e.g., PI, are employed, are not effective in suppressing the CMV and maintaining the capacitor voltage balance simultaneously. To solve the multiple-objective optimization problems, MPC has been proved itself as one of the best solutions and widely used in the field of power electronic converter control recently [15]. So far, most MPC studies applied to multilevel converter control are based on one-step-ahead prediction. This is due to the fact that the MPC is always used for quick dynamic control loops, i.e., current control-loop. Hence, minimizing computational time to achieve quick dynamic response is the priority goal. Recent studies on MPC [16-18] show that multi-step MPC, where predictive horizon is extended, has a significant benefit in improving the steady-state performance in comparison with the one-step-ahead prediction. However, a long predictive horizon for multilevel converter yields large computational cost which causes difficulty in practical implementation [19].

This research focuses on the control design of three phases T-Type converter in grid-connected mode, in which the multiple-step MPC is used as the current controller. The controller not only minimizes the inductor current tracking error but also considers other goals such as minimal CMV, optimal switching sequence, and capacitors voltage balance by modifying the cost function. In addition, the sphere decoding algorithm (SDA) is also employed to reduce the computational time of the multi-step MPC. Numerical simulations show that the proposed multiple-step MPC is better than the one-step counterpart in terms of steady-state performance.

2. System Description

2.1 Designing current controller

The block diagram of the proposed T-Type converter control system in grid-connected mode is illustrated in Fig. 1. Basically, this is a dual-loop control system, in which a conventional PI controller is employed to regulate the DC bus voltage, and a multiple-step MPC is used for the inner-loop to deal with multiple objective optimization problems as discussed above. By modifying the cost function and utilizing SDA method, the number of candidate voltage vectors used for the cost function optimization decline significantly. Thus, make the algorithm possible to be implemented by micro-controllers. A synchronous reference frame phase locked loop (SRF- PLL) [20] is employed guarantee that the generated current is synchronized with the grid.

2.2 Current controller design

The multi-step MPC design for the inductor current loop is divided into four main steps as shown in Fig.2:

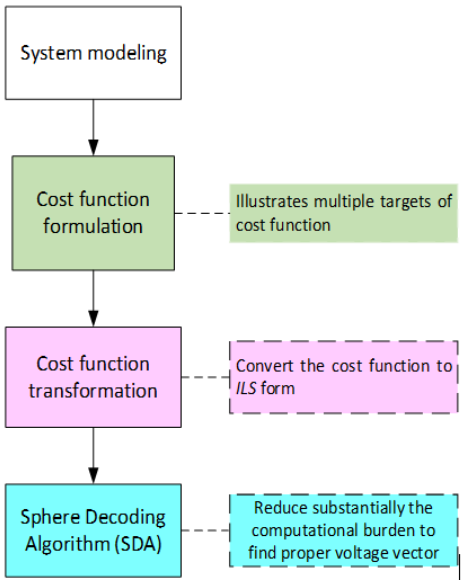


Fig. 2. Multi-step MPC for current controller

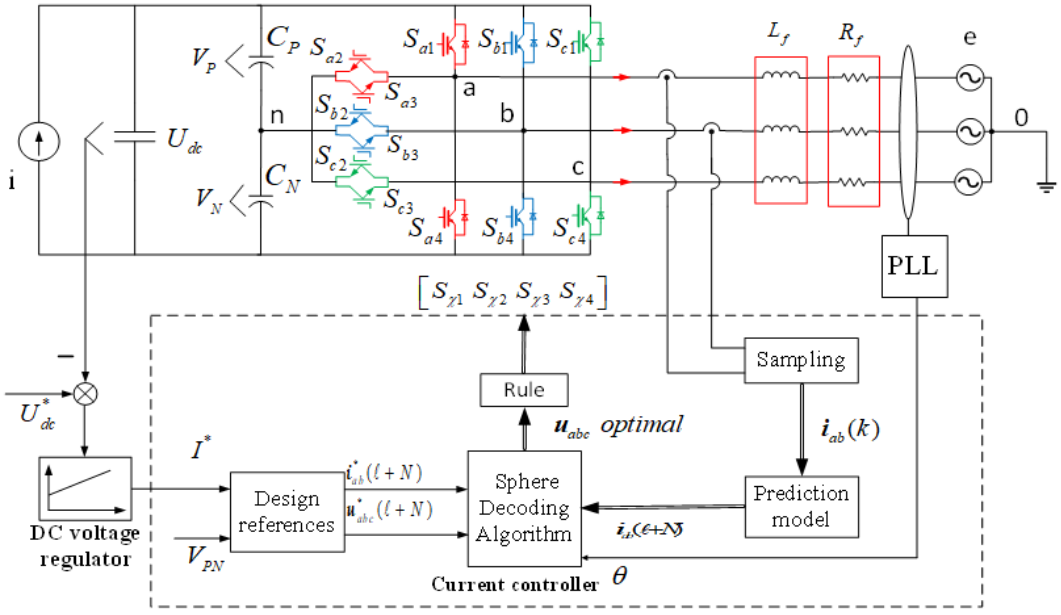


Fig. 1. Control structure for three-phase T-Type inverter in grid-connected mode using Multi-step MPC strategy

2.2.1 System modeling

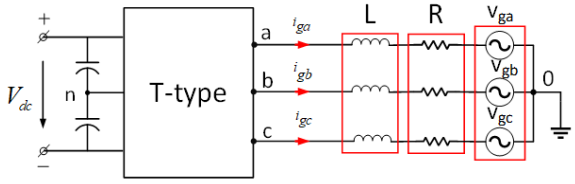


Fig. 3. Grid- connected model with L filter

First, a mathematical model which reflects the behavior of the converter exactly is built. In the continuous-time domain, the converter can be described by the following equations:

$$\begin{cases} \dfrac{di_{ga}(t)}{dt} = -\dfrac{R}{L}i_{ga} + \dfrac{1}{L}\left(v_{an}(t) - v_{ga}(t) - v_{0n}(t)\right) \\ \dfrac{di_{gb}(t)}{dt} = -\dfrac{R}{L}i_{gb} + \dfrac{1}{L}\left(v_{bn}(t) - v_{gb}(t) - v_{0n}(t)\right) \\ \dfrac{dv_{ga}(t)}{dt} = -\dfrac{\omega_g}{\sqrt{3}}v_{gb}(t) + \dfrac{\omega_g}{\sqrt{3}}v_{gc}(t) \\ \dfrac{dv_{gb}(t)}{dt} = -\dfrac{\omega_g}{\sqrt{3}}v_{gc}(t) + \dfrac{\omega_g}{\sqrt{3}}v_{ga}(t) \end{cases}$$

In which, i_{ga}, i_{gb} v_{ga},v_{gb} are the phase current and voltage, respectively. The remaining phase quantities are: $i_{gc} = -i_{ga} - i_{gb}$ and$v_{gc} = -v_{ga} - v_{gb}$. Whilst the angular frequency ω_g is computed by $\omega_g = 2\pi f_g$, where $f_g$is the grid voltage frequency. The equivalent resistor of the capacitors and the inductors are neglected in most high-power systems. For convenience, control inputs and outputs are presented in vector form as following:

$$\begin{cases} x = [i_{ga} \quad i_{gb} \quad v_{ga} \quad v_{gb}]^T \\ u = [u_a \quad u_b \quad u_c]^T u \in \{-1,0,1\} \\ y = i_{gab} = [i_{ga} \quad i_{gb}]^T \end{cases} \quad (1)$$

Suppose that the three-phase voltages are balanced, which means that: $v_{0n}(t) = \frac{1}{3}(v_{an}(t) + v_{bn}(t) + v_{cn}(t))$. Then, equation (1) then can be rewritten in state-space model as:

$$\begin{cases} \dfrac{dx(t)}{dt} = A'x(t) + B'u(t) \\ y(t) = Cx(t) \end{cases} \quad (2)$$

In (3), matrices A' and B' are given in the appendix. Appling Forward- Euler discretization with a sampling period T_s to (3), it gives:

$$\begin{cases} x(k+1) = Ax(k) + Bu(k) \\ y(k+1) = Cx(k+1) \end{cases} \quad (3)$$

where $A = I_4 + T_sA'$ *and* $B = T_sB'$

2.2.2 Cost function design

The general form of the cost function is given in 2nd-order

Euclidean on the 0abc coordinate system as follows:

$$J_N(k) = \sum_{l=k}^{k+N-1} \begin{pmatrix} \|y(\ell+1) - y^*(\ell+1)\|_2^2 \\ +\sigma_u\|u(\ell) - u^*(\ell)\|_2^2 \end{pmatrix} \quad (4)$$

Where $\ell = \{k, k+1, \ldots k+N-1\}$,

$$u(\ell) = [u_a(l) \quad u_b(l) \quad u_c(l)]^T$$
$$y(\ell+1) = [i_a(\ell+1) \quad i_b(\ell+1)]^T$$

The cost function then can be represented in matrix form as:

$$J_N(k) = \|Y(k) - Y^*(k)\|_2^2 + \sigma_u\|U(k) - U^*(k)\|_2^2 \quad (5)$$

In which, the predictive output current matrix **Y(k)** is:

$$\begin{aligned} & y(\ell+1) = Cx(\ell+1) \\ & = CA^{\ell-k+1}x(k) + [CA^{\ell-k}B \quad \ldots \quad CA^0B]U(k) \\ & \Rightarrow Y(k) \\ & = [(y^*(k+1))^T \quad (y^*(k+2))^T \quad \ldots \quad (y^*(k+N))^T] \\ & = \Gamma x(k) + \Upsilon U(k) \end{aligned} \quad (6)$$

The reference output current can be expressed by:

$$\boldsymbol{y}^*(k) = \boldsymbol{i}_{ab}^*(k) = \begin{bmatrix} I^* \sin(2p\,fkT_s + f^*) \\ I^* \sin(2p\,fkT_s + f^* - 2p/3) \end{bmatrix} \quad (7)$$

Where I^* is computed by the DC bus voltage controller and $\phi^*$is determined by the SRF-PLL. Consequently, the reference current vector is

$$\begin{aligned} & Y^*(k) \\ & = [(y^*(k+1))^T \quad (y^*(k+2))^T \quad \ldots \quad (y^*(k+N))^T] \end{aligned} \quad (8)$$

The vector of control voltage $\boldsymbol{U(k)}$ which must be found is

$$\begin{aligned} & U(k) \\ & = [(u(k))^T \quad (u(k+1))^T \quad \ldots \quad (u(k+N-1))^T] \end{aligned} \quad (9)$$

Multiple objectives such as capacitors voltage balance, common-mode voltage minimization, switching optimization...can be included in the cost function by designing the reference control input vector:

$$u^*(\ell) = [u_a^*(\ell) \quad u_b^*(\ell) \quad u_c^*(\ell)] \quad (10)$$

where$\ell \in \{k, k+1, \ldots, k+N-1\}$.

In this research, three approaches to adjusting the reference control voltage vector to achieve the specific goal are:

Method 1: The goal of this method is to minimize the common-mode voltage V_{ON}. According to [19], the reference control input in this case is calculated based on an assumption that $V_{ON} = 0$. In details, by substituting (8) into (1), it gives

$$\begin{aligned} & \frac{d\left[I^* sin(2\pi fkT_s + \varphi_\chi)\right]}{dt} \\ & = -\frac{R_f}{L}.\left[I^* sin(2\pi fkT_s + \varphi_\chi)\right] \\ & -v_{gx} + V_{dc}.u_\chi^*(k) \\ & \Rightarrow u_\chi^*(k) = \frac{R_f I^*}{V_{dc}} sin\left(2\pi fkT_s + \phi_\chi\right) \\ & + \frac{2\pi fLI^*}{V_{dc}} cos\left(2\pi fkT_s + \phi_\chi\right) + \frac{v_{gx}}{Vdc} \end{aligned} \quad (11)$$

where

$$\phi_a = 0,$$
$$\chi \in \{a, b, c\}, \phi_b = 2\pi/3,$$
$$\phi_c = -2\pi/3$$

❖ Method 2: Switching optimization

In term of optimizing the number of switching sequence the reference of control input of the two consecutive sampling cycle should be the same, which means:

$$U^*(k) = Uopt(k-1) \quad (12)$$

Method 3: DC voltage balance

There are three ways to implement this method:

Sub-method 1: Calculate the reference matrix U*(k) from the continuous-time system model with an assumption that $V_p = V_n$. However, this way requires complicated mathematical equations which increases the computation cost.

Sub-method 2: An interesting property of the T-Type converter is that it is possible to create a voltage vector from two different switching states as shown in Table 1. Which means the system has more degree of freedom to handle other goals.

Table 2. Reference value for control input in method 3

Reference value	Energy injected to grid		Energy taken from grid	
$u^*(k) = u^*(k+1) = \ldots = u^*(k+N-1)$	$V_p > V_n$	$V_p < V_n$	$V_p > V_n$	$V_p < V_n$
	$[111]^T$	$[-1\ -1\ -1]^T$	$[-1\ -1\ -1]^T$	$[111]^T$

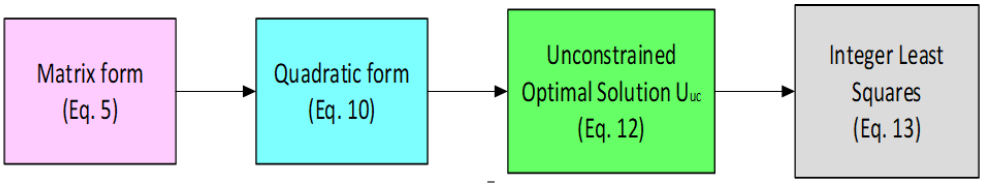


Fig. 4. Four steps to transform the cost function

Table 1. Redundant states of small voltage vectors

Positive redundant states	Negative redundant states
[1, 0, 0]	[-1, 0, 0]
[0, 0, 1]	[0, 0, -1]
[0, 1, 0]	[0, 1, 0]
[1, 1, 0]	[-1, -1, 0]
[0, 1, 1]	[0, -1, -1]
[1,0, 1	[-1,0, -1]

Particularly in this case, with the same chosen voltage vector, either positive or negative redundant states can be selected depending on the difference between the two capacitors voltage.

Sub-method 3: This is also one of our main contributions in this research, focusing on capacitor voltage balance. In our proposed method, not only the difference between the two capacitors voltage, but also the power transferred direction is considered to properly select the switching state. In details, if the power is transferred to the grid and $V_P > V_N$, the corresponding positive redundant states are selected because the existing of state '1' helps discharge C_p and charge C_n. In other words, $u^*(k) = [111]^T$ is the best solution to recover the voltage balance in this case and should be chosen as the reference. Similarly, if $V_p < V_n$, the reference control input

vector is chosen as: $u^*(k) = [-1\ -1\ -1]^T$. For reverse power flow, i.e., from grid line to the DC link, the selection of the reference $\boldsymbol{u^*}$ is inversed. Table 2 summarizes the reference values for sub-method 3. In comparison with sub-method 2, a remarkable advantage of our proposed method is that the capacitor voltage balance is integrated as a part of the cost function which allows the designer to tune its weighting factor.

2.3.3. Cost function transformation

Substituting (6) into (5), the quadratic form of the cost function is:

$$J_N = U(k)^T W U(k) + 2F(k)^T U(k) + \varepsilon(k) \quad (13)$$

By solving the partial derivative equation: $\frac{\partial J_N}{\partial U} = 0$, the vector of control signal that minimize the cost function is:

$$U_{uc} = -W^{-1}F(k) \quad (14)$$

Then, by substituting (11) into (10), the extreme point of (10) in every consecutive sampling cycle is computed by:

$$J_N(k) = \|U(k) - U_{uc}(k)\|_W^2 \quad (15)$$

Conventionally, only the first element of (11) is applied to the power stage. And this control voltage is generated by the state vector modulation (SVM) technique. To utilize the redundant states of the T-Type converter, the SVM is substituted by a searching algorithm which finds the switching state that minimize the extreme point (12). The algorithm also employs the SDA to lower the computational time by reducing the candidate of switching states in each sampling cycle.

- *Integer Least Squares - ILS*

Since **W** is a symmetric and positive definite matrix, (16) can be reformulated as an ILS-problem by performing the Cholesky decomposition to $\boldsymbol{W^{-1}}$, following that:

$$\boldsymbol{W^{-1} = H^{-1}\ H^{-T}} \quad (16)$$

In which, $\boldsymbol{H}$ is a unique invertible lower triangular matrix satisfying:

$$\boldsymbol{W = H^T H} \quad (17)$$

As a result, the cost function (12) can be reformulated in term of $\boldsymbol{H}$ as:

$$J_N(k) = \|HU(k) - \tilde{U}_{uc}(k)\|_2^2 \quad (18)$$

where $\tilde{U}_{uc}(k) = HU_{uc}(k)$ is considered as the center of the created sphere. Therefore, the cost function has been transformed from the radius of an ellipse to the radius of a sphere with a fixed center point during each sampling period, and the SDA method can be applied in the final step.

2.3.4 SDA method

The flow chart in Fig. 5 shows how to implement the SDA [19] in our research.

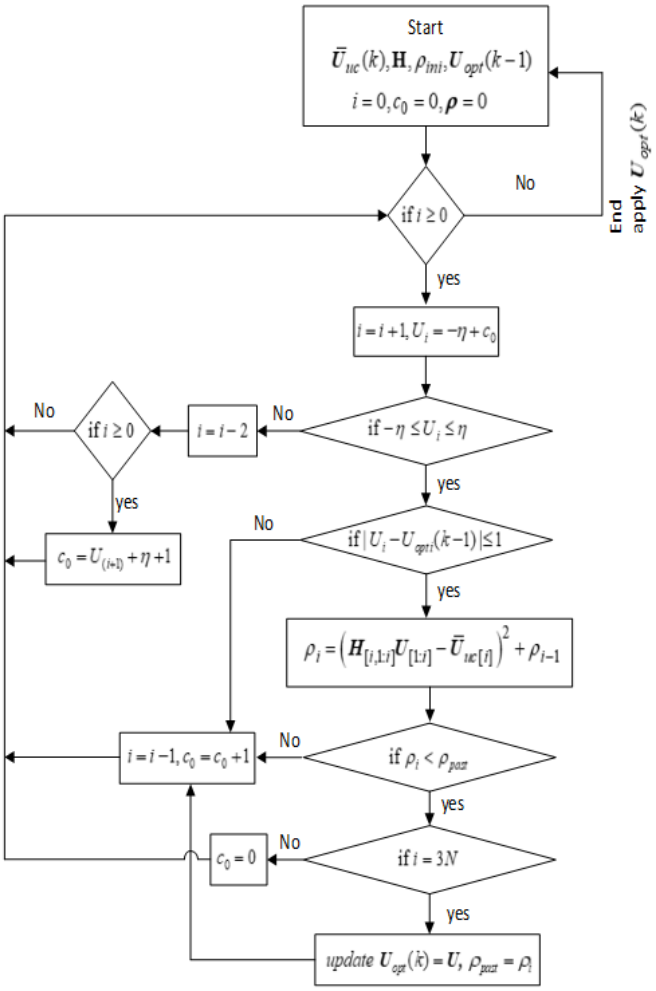


Fig. 5. SDA algorithm

An initial radius is selected and continuously compared with the calculated value of the cost function corresponding to the voltage vectors. Since **H** is a diagonal matrix, the calculated radius is sum of squares, so the vector exclusion is implemented by row and column, thereby significantly reducing the computation burden.

3. Simulation Results

In this section, various numerical simulations are conducted to show the effectiveness of the proposed method, as well as appropriately choose the number of prediction steps. Comparative analysis to show the advantages of the multi-step MPC over the one-step-ahead MPC is also carried out. The parameters used in simulation are provided in Table 3.

Table 3 Simulation parameters

Power circuit parameters	
Input DC capacitor C_N	$470uF$
Input DC capacitor C_P	$470uF$
Filter inductor L_f	$6\ mH$
Switching frequency f_s	$20\ kHz$
Weighting factor: σ_u	0.14
Controller parameters	
PLL parameters: Kp=0.2 Ki=38	
Voltage controller parameters: Kp=28.4 Ki=400	

The performance of the proposed control strategy is evaluated in both steady-state and transient-state. In detail, the power transferred is kept constant in the first 0.1s, and then suddenly changed by increasing the injected current abruptly, i.e., from 15A to 25A.

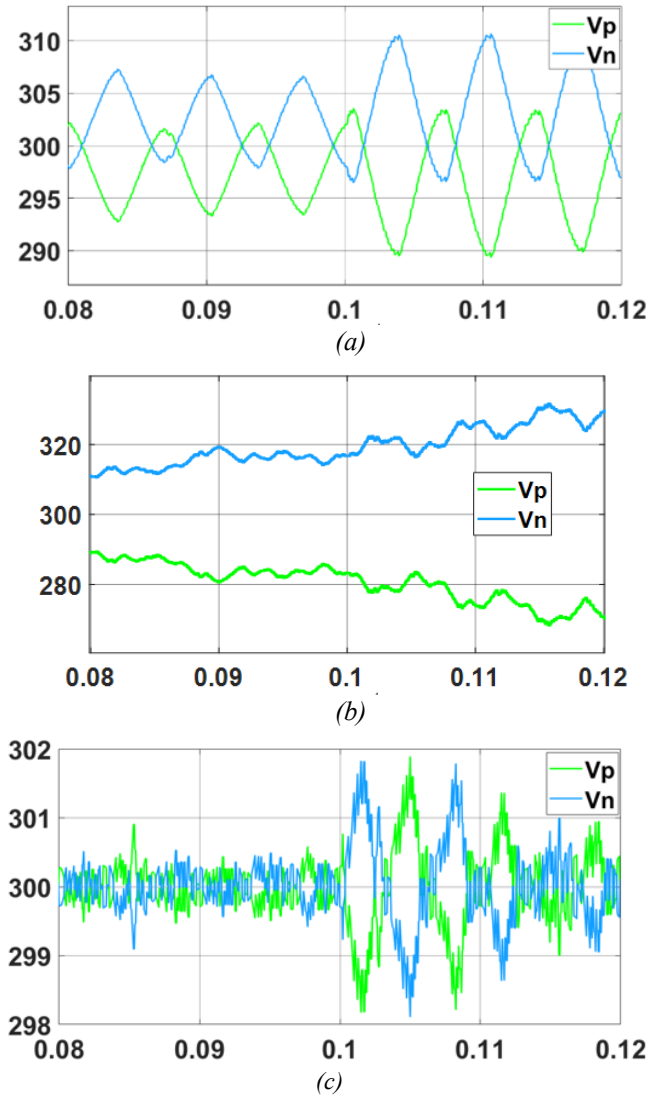


Fig. 6. Voltage balance on 2 input DC capacitors
a) Method 1; b) Method 2; c) Method 3

First, the capacitor voltage balance between our proposed method, i.e., method 3, and the two others, i.e., method 1 and method 2, are compared. It can be seen from Fig. 6c that the proposed method gives the best performance since the difference between V_P and V_N is just below 4V. In contrast, the amplitude of voltage imbalance of method 2 is much larger, i.e., 20V as shown in Fig. 6.a. Particularly, Fig. 6b shows that method 3 even yields voltage imbalance since the difference $\Delta V_c = V_P - V_N$ tends to increase over time.

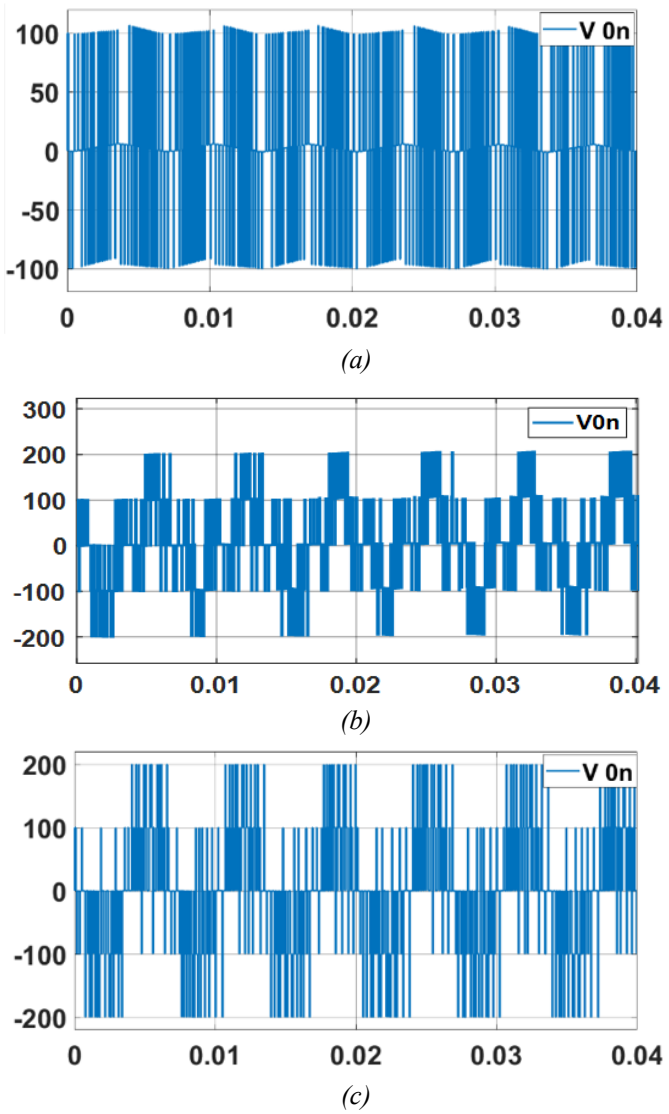


Fig. 7. The common-mode voltage V_{ON}
a) Method 1; b) Method 2; c) Method 3

Figure 7 presents the ability to minimize the CMV of the 3 above mentioned methods. As can be observed in Fig. 7a, the first method gives the smallest CMV, not our proposed method. This result is obvious since our proposed method only focuses on capacitor voltage balance.

As discussed previously, the multi-step MPC can give a better performance over the conventional one-step-ahead MCP in steady-state. The problem is how many steps should be chosen to negotiate between the expected performance and the computational cost. Hence, simulations to show the relation between the total harmonic distortion (THD) of the grid-connected current, and the number of prediction steps are conducted. As can be seen in Fig. 8, the THD tends to decrease as the number of predictions N increases. However, the THD is kept constant as the number of predictions is sufficiently large. In this specific case, N=4 is chosen for the next simulations since it gives a similar performance as the case where N>4, while the computational effort is much less, i.e., 27 times smaller than the case where N=5.

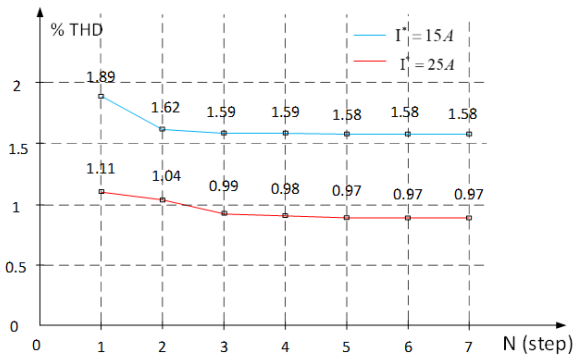


Fig. 8. THD of the grid-connected current vs the number of prediction steps

With N = 4, simulations to show the performance of the multi-step MPC are carried out. The steady-state performance of the d-axis current is shown in Fig. 9. As N = 4, the tracking performance of the MPC is better than when N = 1 in terms of accuracy as well as the amplitude of the current ripple.

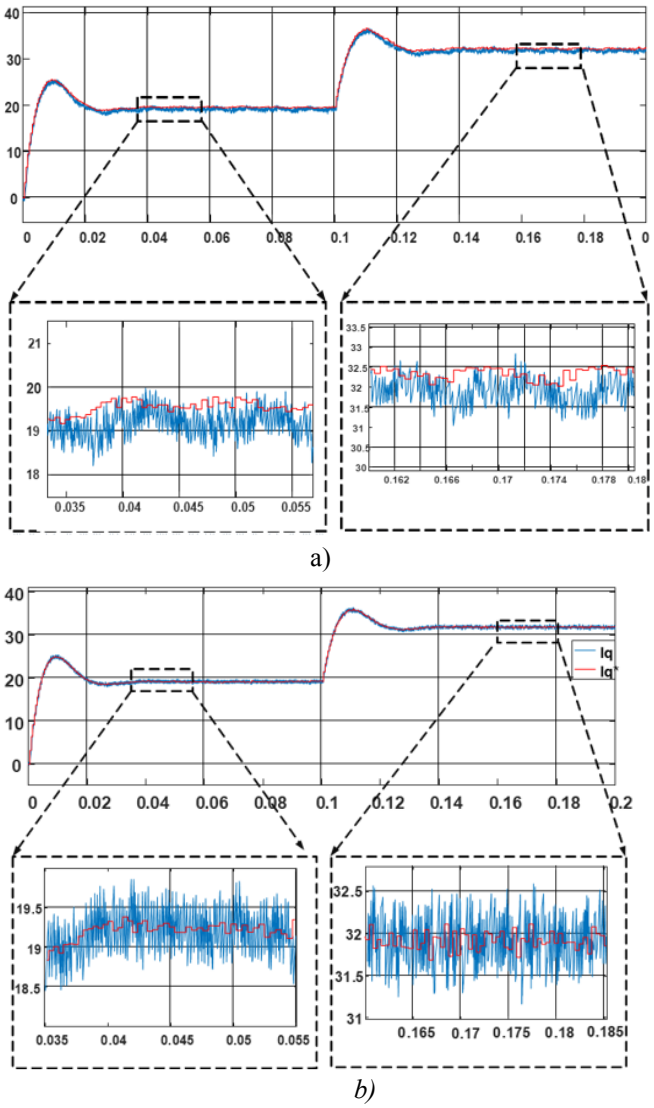


Fig. 9. Performances of current Id
a) N = 1; b) N = 4

The dynamic of the multi-step MPC is shown in Fig. 10. In both cases, i.e., N = 1 and N = 4, the transient responses are the same, just about 0.25ms. This quick response helps improve the dc bus voltage regulator since the power transfer can be quickly performed.

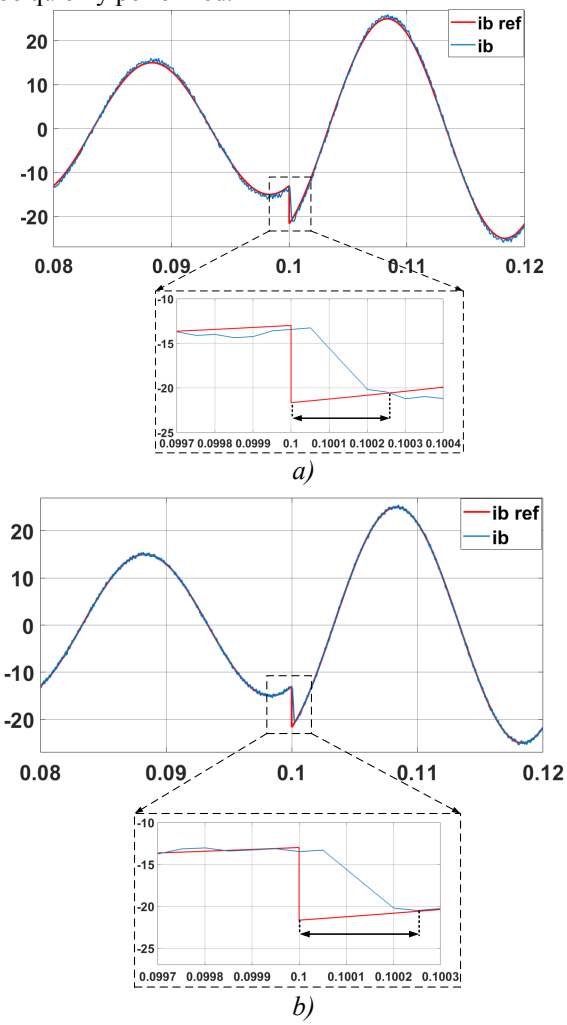
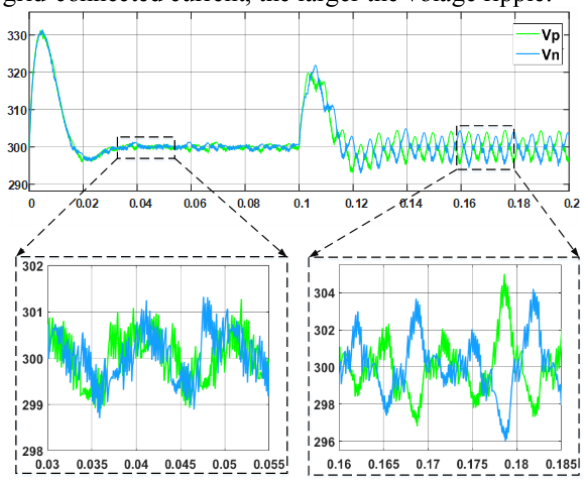


Fig. 10. Dynamic performance of the grid-connected current
a) N =1; b) N =4

It can also be observed from Fig. 11 that the variation of the prediction step N does not affect the capacitor voltage balance The difference between V_P and V_N is only governed by the amplitude of the grid-connected current. Obviously, the larger the grid-connected current, the larger the volage ripple.



(a)s

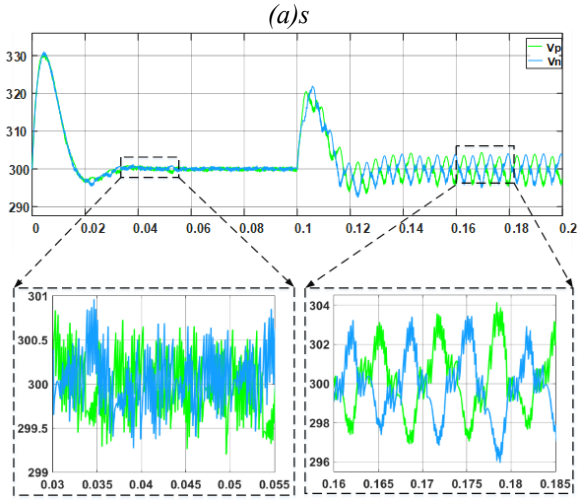


Fig. 11. Voltage balance on 2 input capacitors
a) N = 1; b) N =4

Finally, the efficiency of the spherical decoder algorithm is evaluated. In comparison with the conventional method which tries all voltage vectors to find the optimal solution, the SDA reduces the computational cost significantly by reducing the candidate of scanned vectors. Figure 12 shows the average cycle that SDA uses in each sampling period to solve the optimization problem (13). As can be seen, the SDA takes only 1240 cycles, on average, to get the optimal solution. In contrast, scanning all vectors with the T-Type topology may take up to 3^{3N} cycles to get the solution, i.e., 531441 cycles with the number of prediction N = 4.

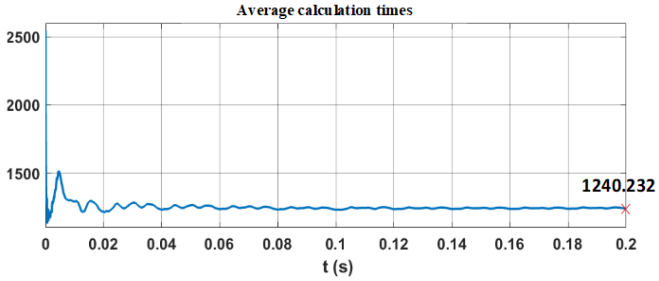


Fig. 12. Computational times in one sample time T_s

Conclusion

In this research, the application of the multi-step MPC to the T-type converter in grid-connected mode is discussed. Two main contributions are offered to improve the control system performance. First, a modification is made to improve the capacitor voltage balance. Instead of directly selecting the redundant switching states as usual, a multi-objective cost function is proposed in which the capacitor voltage balance is regarded as one of the goals with a tunable weighting factor. Second, the spherical decoder algorithm is successfully applied to the MPC to significantly reduce the computational cost in each sampling cycle. Hence, makes the algorithm possible to be implemented by commercial microcontrollers. Various numerical simulations are conducted to verify the effectiveness of the proposed method. The results show that all the goals set are achieved, i.e., lower THD and smaller capacitor voltage imbalance. Besides, comparative results also show that multi-step MPC gives better performance than the one-step-ahead MPC in terms of tracking accuracy.

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Appendix

$$A' = \begin{bmatrix} 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f R} & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f R} \end{bmatrix}$$

$$B' = \frac{V_{dc}}{6L}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

$$x = \begin{bmatrix} i_{fa}(k) \\ i_{fb}(k) \\ v_{Ca}(k) \\ v_{Cb}(k) \end{bmatrix}, \Gamma = \begin{bmatrix} CA \\ CA^2 \\ \vdots \\ CA^N \end{bmatrix}$$

$$\Upsilon = \begin{bmatrix} \boldsymbol{CB} & \boldsymbol{0} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{CAB} & \boldsymbol{CB} & \cdots & \boldsymbol{0} & \boldsymbol{0} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \boldsymbol{CA^{N-1}B} & \boldsymbol{CA^{N-2}B} & \cdots & \boldsymbol{CAB} & \boldsymbol{CB} \end{bmatrix}$$

$W = \Upsilon^T \Upsilon + \sigma_u I_{\varsigma}$,
$F(k) = \Upsilon^T \Gamma x(k) - \Upsilon^T Y^*(k) - \sigma_u U^*(k)$,
$\varepsilon(k) = \|\Gamma x(k) - Y^*(k)\|_2^2 + \sigma_u \|U^*(k)\|_2^2$