


H5-ZVR Single-Phase Grid-Tied Inverters for Photovoltaic Application

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Abstract- The majority of companies are shifting to renewable energy sources as non-renewable fuels are increasingly depleting. Solar energy is a dependable form of green energy. The solar energy after converting to AC through an inverter it is possible to inject into the grid to support distributed power generation system. Transformerless grid-tied inverters have become popular due to their lightweight and reduced cost. The leakage current does exist in this kind of inverter that deteriorate the performance of the inverter. This paper presents a novel H5-ZVR, H5-ZVRD and H5-ZVRS topologies to address the leakage current issue. These inverters take the benefit of hybrid technology, where H5 inverters are integrated with HB-ZVR topologies. To operate the inverter at its highest performance an appropriate hybrid pulse width modulation is also presented. The inverters are simulated in MATLAB to verify the operation and it is found that the leakage current of the inverters is considerably reduced as compared to HB-ZVR topologies. The leakage current of H5-ZVR, H5-ZVRD and H5-ZVRS are found to be 10 mA, 7.3 mA and 7.3 mA respectively and THD of these modules are 1.03%, 0.91% and 0.91% respectively. Also, the topologies present good common mode and differential mode characteristics.

Keywords Grid-tied, single-phase, neutral point clamping, leakage current, full-bridge, transformerless, total harmonic distortion, photovoltaic.

1. Introduction

The term "Distributed Generation" refers to the generation of power for on-site use rather than distributing energy from a large, centralised system through the electric grid [1-2]. Decentralized generation occurs when electricity is produced and transmitted using small-scale technology closer to the end users. These distributed generation systems, while not limited to, are primarily based on renewable technology such as wind turbines, photovoltaic cells, geothermal electricity, and micro hydropower plants [3-4]. A grid-tie inverter (GTI) is a type of power converter that converts direct current (DC) to alternating current (AC) and works in tandem with a power grid, typically at 120 V_{rms} at 60 Hz or 240 V_{rms} at 50 Hz. The DC voltage is typically produced by photovoltaic modules or batteries. GTIs enables renewable energy systems to be connected to the grid. A GTI converts DC voltage from solar

cells or photovoltaic panels to alternating current (AC) voltage that is compliant with the power grid. When the grid goes offline, it can immediately cease providing electricity to the power lines. A GTI will fuel our home and also pump surplus energy back into the grid, lowering the electric bill.

Some of the challenges faced by GTI's are low insulation impedance, solar grid-tie inverters common faults, leakage current fault, DC overvoltage protection. The drawbacks of traditional inverters or DC/AC converters have been overcome by multilevel inverter topologies. Low switching frequency, low dv/dt, heavy power leakage, and high electromagnetic interference are some of the key drawbacks of traditional inverters. Multilevel inverters generate common-mode voltage, which eliminates load tension, input current distortion is minimal in multilevel inverters. The multilevel inverter is capable of operating at all fundamental switching frequencies. Switching stress on power devices are

reduced and reliability is increased as the switches operate at a lower switching frequency in the multilevel inverters. The combination of a selective harmonic removal technique and a multilevel topology yields an output waveform with low overall harmonic distortion without the use of a filter circuit.

A modified carrier-based PWM technique is presented in the paper [5] to reduce the leakage current. The suggested modulation strategy is contrasted with the traditional technique and is simulated to verify the effect of the leakage current in a changed carrier dependent PWM. The system is efficient in leakage current minimization. The voltage and current THD values are less than 8% and 5% respectively. In [6] an inverter with boosting ability and common ground feature is presented. In this maximum current controller technique is employed to unlock power switch gates and track both active and reactive powers. The grid's null and the negative terminal of the photovoltaic panels are grounded, which addresses the common mode leakage current problem. An inverter that operates at twice the switching frequency is presented in [7] which helps in operating the switches at half of the required output frequency. This intern reduces the common-mode leakage current, switching stress on the power devices. A five-level inverter is proposed in [8]. Here common-mode voltage is clamped to half of the photovoltaic voltage. As a consequence, the high-frequency common-mode voltage is deactivated and the leakage current is reduced.

Mitigation of ground leakage current of single-phase PV inverter using hybrid PWM with soft voltage transition and nonlinear output inductor is proposed in [9]. Since it doesn't require a massive, pricey and low isolation transformer, transformerless full-bridge voltage source inverter is favoured in mitigation of ground leakage current of single-phase inverter using hybrid PWM. To mitigate ground leakage current caused by high frequency (HF), the switching of switches in the full-bridge is a critical design consideration especially in installations with high parasitic capacitance. To diminish ground leakage current, a virtual ground (VG) method is used in this topology. To profile the output current and prevent sudden changes in the common-mode voltage, a hybrid PWM technique is taken into action, and a nonlinear output inductor is used to diminish the current ripple. In [10] novel single-stage transformer-less cascaded differential boost single-phase photovoltaic inverter for grid-tied applications is mentioned. In this paper, by cascading a two-switch boost converter and a four-switch buck-boost converter with two switches shared, a single-stage transformer-less inverter is recommended, which removes the need for an output filter and thereby reduces the part count. It makes use of boost and buck-boost modules connected in various ways. The operation of the suggested topology is shown by the two modes listed below. Mode I (0 t DTs), Mode II (0 t DTs) (DTs t Ts). As compared to current topologies, the proposed topology's loss distribution of all switches is less at various loading conditions, and it is discovered that the proposed topology's output is better at all loading conditions.

The multi-sampling method for single-phase grid-connected cascaded H-bridge inverters is presented in [11] is a multi-sampling approach that uses the shortest sampling interval to sample current and voltage without acknowledging

the current ripple generated by the switching. Rectifying, significantly eliminates time delay and increases the bandwidth of the closed-loop control mechanism, leading to a multi-sampling process for single-phase grid-connected CHB multilevel converters modulated by PSC-PWM. A Single-phase grid-tied transformer-less inverter with zero leakage current for a PV system is presented in [12]. This topology involves, the configuration of a device that includes a 5L-NPC inverter with a control technique that retains the required voltage balance for the input DC-link of a transformer-less grid-tied single-phase PV system. It allows for zero leakage current and the potential to minimize harmonic content as a function of performance as opposed to lower MLIs.

In photovoltaic cells, a stray or parasitic capacitance exists between the photovoltaic cell and the earth ground. When photovoltaic cells are used to generate power in a distributed power generation system a leakage current flows between the grid and photovoltaic cell. Hence, isolation must be provided between the grid and the photovoltaic cell to avoid the flow of this leakage current as it produces electromagnetic interference and also it is hazardous. The stray capacitance is dependent on various atmospheric conditions and may vary up to 150 nF/kW [13]. A low-frequency transformer is used as an isolator to avoid the leakage current. The insertion of the line transformer makes the inverter bulkier, heavy and expensive. Hence, the line transformer is removed in the grid-tied inverter system. The removal of the transformer must be compensated with a suitable galvanic isolation technique to reduce the leakage current. DC bypass and AC bypass are two such techniques that can individually be used to avoid or reduce the flow of leakage current.

An H5 inverter [14] and its derivatives are the grid-tied inverters that use the DC-bypass technique to avoid the flow of leakage current between the grid and the photovoltaic cell. H5 is a full-bridge inverter with four power switches $S_1 - S_4$ and a fifth switch is connected between the photovoltaic cell and the full-bridge to achieve DC-bypass as shown in Fig. 1a. The gating signals are applied to power switches such that during freewheeling mode the fifth switch disconnects the photovoltaic cell from the inverter and hence from the grid. Unipolar or hybrid SPWM switching sequences can be used to excite the power switches in the H5 inverter. This is a simple and effective method of providing isolation. However, the leakage current varies at switching frequency and also as the current flows through this additional switch during active modes the power loss increases and hence reduces the efficiency.

The highly efficient reliable inverter concept (Heric) and its derivatives use a technique of AC-bypass to reduce the leakage current. Heric model also consists of a full-bridge with four switches $S_1 - S_4$. An additional switches S_5 and S_6 are added at the inverter output as referred to in [15]. In AC-bypass the freewheeling current flows through these two switches and avoids current to reach the photovoltaic cell thereby disconnects the photovoltaic cell from the grid. As there are no additional switches in the path of active mode current this inverter is more efficient than the H5 inverter. In its improved version known as Enhanced Heric inverter presented in [16] the high-frequency component in the leakage

current is removed with the help of a hybrid switching cell consisting of six diodes $D_1 - D_6$ and a switch S_5 as shown in Fig. 1c. This inverter works with a Unipolar SPWM signal. This circuit also comes under another popular inverter known as HB-ZVR proposed in [17]. The circuit diagram of FB-ZVR

is as shown in Fig. 1b. The Enhanced Heric is also known as HB-ZVRD topology is derived by adding diode D_6 as shown in Fig. 1c into the HB-ZVR inverter. The third derivative of HB-ZVR is obtained by replacing D_5 with a power switch to form HB-ZVRS [18]. All the topologies outperform

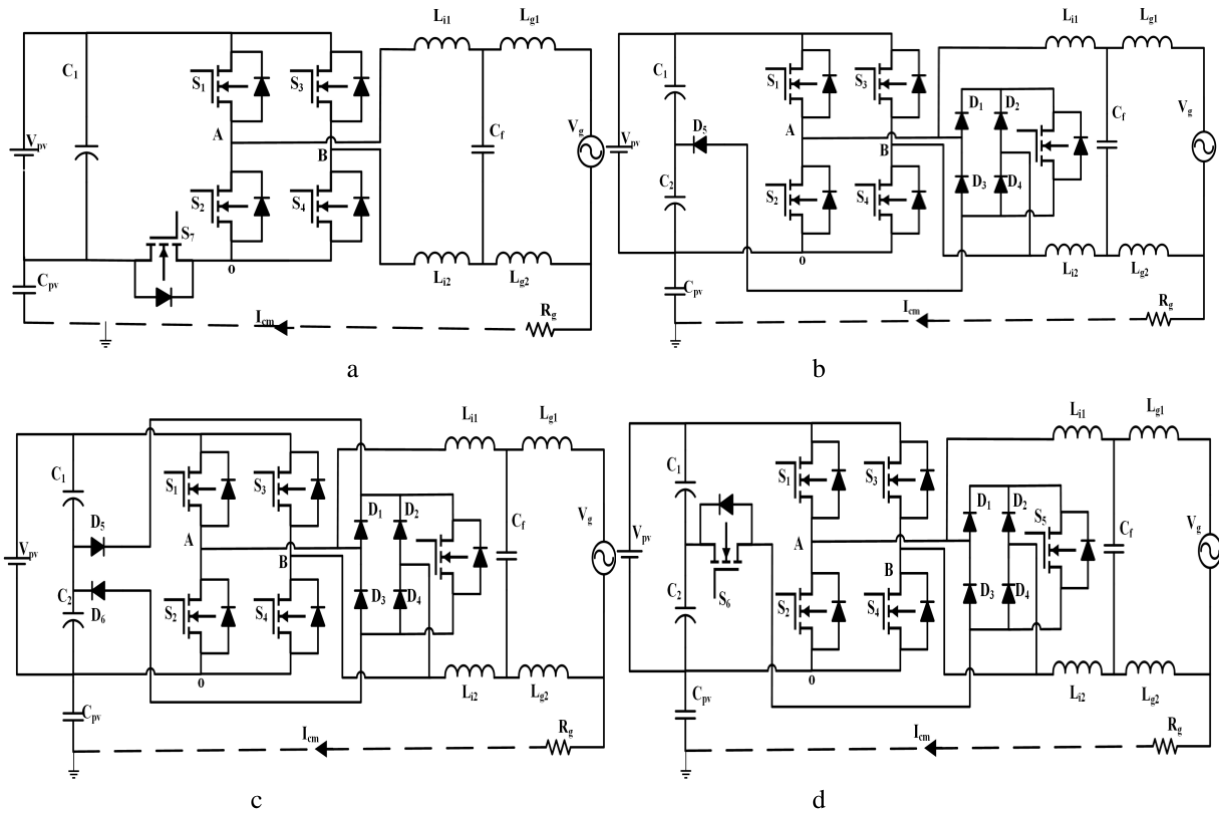


Fig. 1 a. H5 Inverter b. HB-ZVR c. HB-ZVRD d. HB-ZVRS

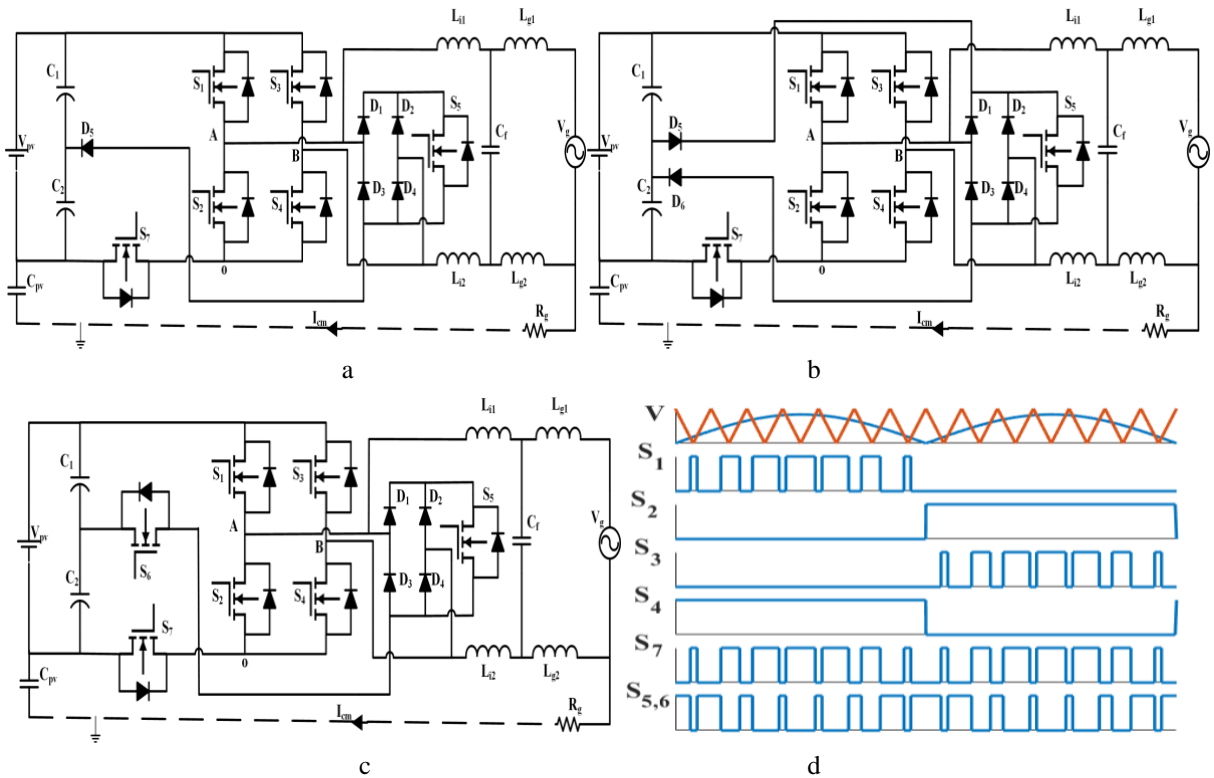


Fig. 2. Proposed Topologies a. H5-ZVR b. H5-ZVRD c. H5-ZVRS b. Gating Signal

concerning common mode and differential mode characteristics but still, to reduce the leakage current further this paper presents novel H5-ZVR topologies.

In the rest of the paper Section 2 in the paper describes proposed topologies. In section 3 explanation of the LCL filter is given. In Section 4 simulation results are discussed along with a comparison of the multilevel inverters and the conclusions obtained are presented in section 5.

2. Proposed Topologies

To take advantage of both DC-bypass and AC bypass techniques this paper presents a novel method to reduce leakage current in the inverter by fusing DC-bypass and AC bypass to come up with different inverter topologies. It is expected that when the two techniques are merged the results could be better than the one that uses a single technique. Hence, an effort is made here to combine the H5 inverter and HB-ZVR topologies to arrive at new topologies. It is observed that when the HB-ZVR inverter is operated with Hybrid SPWM the leakage current is at a higher level. H5 inverter reduces the leakage current in comparison with full-bridge inverter but still, there are high-frequency fluctuations present in it.

Fig. 2a shows a new single-phase grid-tied inverter based on the proposed methodology. The topology can be named H5-ZVR as it is the combination of H5 and HB-ZVR topologies. This inverter has four switches $S_1 - S_4$ in its full-

bridge and a switch S_7 between the inverter and the photovoltaic cell similar to the H5 inverter. It also contains a ZVR switching cell consisting of switch S_5 and four diodes $D_1 - D_4$ between the filter and the output of the inverter. A similar topology is obtained by adding the HB-ZVRD network into the H5 topology as shown in Fig. 2b. This circuit has an additional diode D_6 . HB-ZVRS is integrated with H5 to develop another topology as shown in Fig. 2c. In this, a switch S_6 is inserted in the place of diode D_5 of the H5-ZVR topology. As unipolar and bipolar SPWM technique doesn't yield the expected output, these topologies are operated with Hybrid SPWM switching signal as shown in Fig. 2d. All inverters work in four different modes. To illustrate the working principle H5-ZVRS shown in Fig. 2c is considered.

a. Mode-I: Positive Active Mode

Mode-I is a positive active mode in which the grid voltage will be at a positive cycle. In this mode S_1, S_4, S_7 are turned ON and S_2, S_3, S_5, S_6 are turned OFF. The current path is $V_{PV}-S_1-V_G-S_4-S_7-V_{PV}$ as shown in Fig. 3a. The voltage V_{AN} is equal to V_{PV} and $V_{BN}=0V$. Hence, the differential mode voltage is

$$V_{AB} = V_{AN} - V_{BN} = V_{PV} - 0 = V_{PV} \quad (1)$$

The common-mode voltage is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{PV} + 0}{2} = \frac{V_{PV}}{2} \quad (2)$$

b. Mode-II: Positive freewheeling Mode

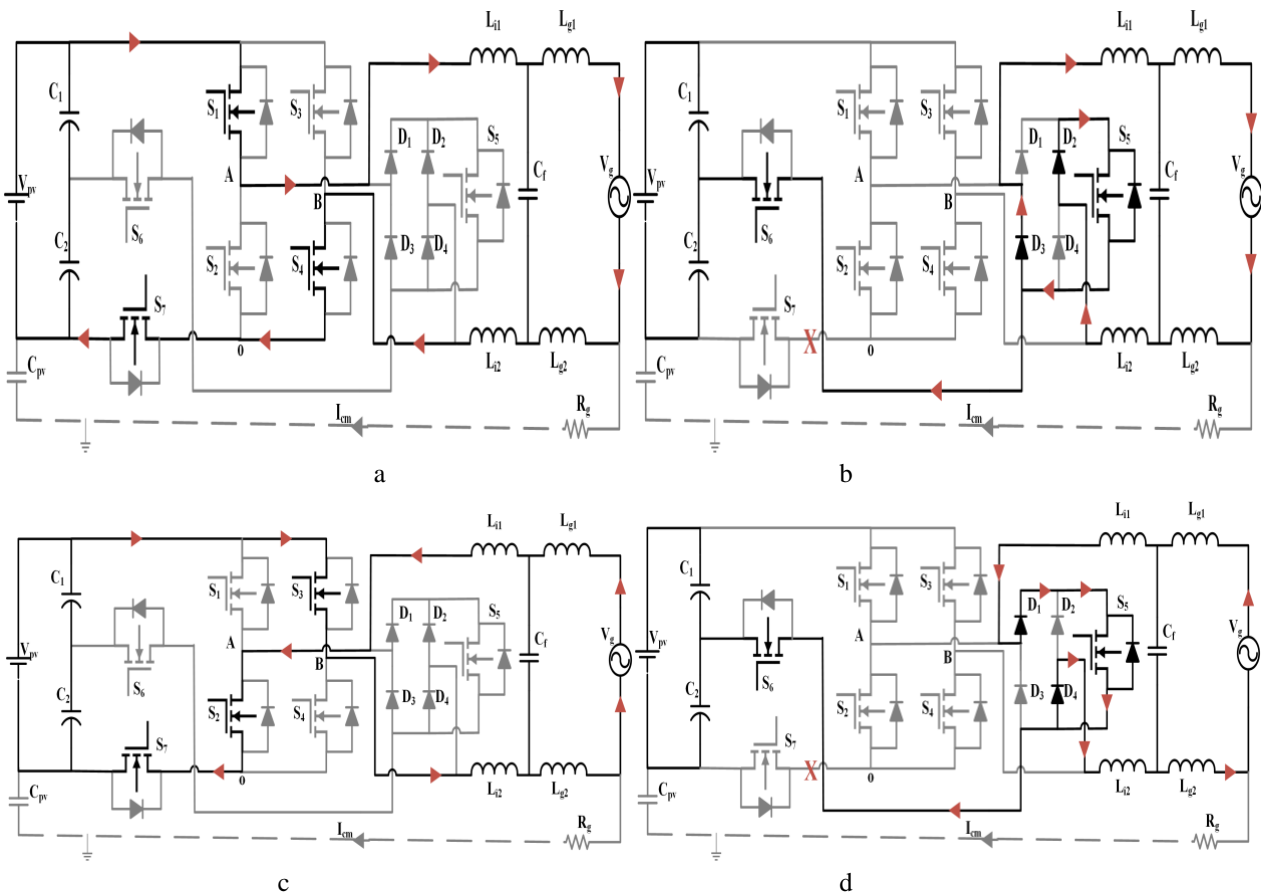


Fig. 3. H5-ZVRS inverter operation in a. Mode-1 b. Mode-2 c. Mode-3 b. Mode-4

Table 1 Switching Status

Mode	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇
I	ON	OFF	OFF	ON	OFF	OFF	ON
II	OFF	OFF	OFF	ON	ON	ON	OFF
III	OFF	ON	ON	OFF	OFF	OFF	ON
IV	OFF	OFF	ON	OFF	ON	ON	OFF

Mode-II is a positive freewheeling mode in which inductor current flows through the freewheeling path. In this mode, S₅, S₆ are turned ON and S₁, S₂, S₃, S₄ and S₇ are turned OFF. The current path is V_G-D₂-S₅-D₃-V_G as shown in Fig. 3b. The voltage V_{AN} is equal to $\frac{V_{PV}}{2}$ and V_{BN} is equal to $\frac{V_{PV}}{2}$. Hence, the differential mode voltage is

$$V_{AB} = V_{AN} - V_{BN} = \frac{V_{PV}}{2} - \frac{V_{PV}}{2} = 0 \tag{3}$$

The common-mode voltage is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{PV}}{2} \tag{4}$$

c. Mode-III: Negative Active Mode

Mode-III is a negative active mode in which the grid voltage will be at a negative cycle. In this mode S₂, S₃, and S₇ are turned ON and S₁, S₄, S₅, S₆ are turned OFF. The current path is V_{PV}-S₂-V_G-S₃-S₇-V_{PV} as shown in Fig. 3c. The voltage V_{AN} is equal to 0V and V_{BN}=V_{PV}. Hence, the differential mode voltage is

$$V_{AB} = V_{AN} - V_{BN} = 0 - V_{PV} = -V_{pv} \tag{5}$$

The common-mode voltage is

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{0 + V_{PV}}{2} = \frac{V_{PV}}{2} \tag{6}$$

d. Mode-IV: Negative freewheeling Mode

Mode-IV is a negative freewheeling mode in which inductor current flows through the freewheeling path. In this mode, S₅, S₆ are turned ON and S₁, S₂, S₃, S₄ and S₇ are turned OFF. The current path is V_G-D₁-S₅-D₄-V_G as shown in Fig. 3d. The voltage V_{AN} is equal to $\frac{V_{PV}}{2}$ and V_{BN} is equal to $\frac{V_{PV}}{2}$. Hence, the differential mode voltage is

$$V_{AB} = V_{AN} - V_{BN} = \frac{V_{PV}}{2} - \frac{V_{PV}}{2} = 0 \tag{7}$$

The common-mode voltage

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{PV}}{2} \tag{8}$$

Table 1 shows the switching status of power devices at different modes.

3. Filters For Grid-Tied Inverter

3a. LCL Filter: As per IEEE STD. 1547 the total voltage harmonic distortion allowed in distributed power generation system is less than 5%. The output of the inverter generally contains harmonics with fundamental frequency and is spread over to switching frequency. Hence it is required to filter the harmonic components present in the output of the filter with a suitable low pass filter. The low pass filter considered for filtering these harmonic components is designed using L, LC or LCL circuits. For the required IEEE STD. 1547 standard it

is found that the LCL filter is more suitable as it reduces the harmonic components significantly [19]. The major problem faced in the design of the LCL filter is damping and resonance at a certain frequency. The damping can be achieved by using passive or active damping methods. It is found that the passive damping method is a simple yet easy technique to reduce the damping while it introduces losses. Active damping is a more suitable technique for effective damping but the system is more complex than passive damping. In the literature, many authors have proposed different methods for calculating resonance frequency. But most of the time it is taken as greater than 10 times the fundamental frequency.

Fig.4. shows the basic structure of the LCL filter. L₁ is an inverter side inductor, L₂ is a grid side inductor, C_f is a filter capacitor and R_d is a damping resistor. The design of L₁, L₂, C_f and R_d values depends on specific requirements of the expected output such as current ripple, filter size, switching ripple attenuation [20]. The converter side inductance is designed to limit the current ripple generated by the inverter that intern depends on the switching frequency of the gating signal. The grid side inductor depends on the acceptable switching ripple by the grid. The filter capacitor affects the power factor hence the power factor needs to be considered while designing the filter capacitor in the LCL filter. The resistor R_d connected in series with filter capacitor acts as a passive damper, provides necessary damping required for the LCL filter.

3b. Steps to find LCL filter component values

This session provides a design technique used for the LCL filter based on the standard requirements.

Step 1: Define the parameters

- Power rating – P_i
- Grid voltage – V_g
- Grid frequency – f_g
- Switching frequency – f_s
- PV voltage – V_{dc}

Maximum ripple current allowed at the output of the filter in percentage– R_i

Step 2: Find the modulation index

$$m = \frac{V_g \sqrt{2}}{V_{dc}} \tag{9}$$

Step 3: Find maximum current ripple

The maximum ripple current is found by using R_i and is given by Eq. (10).

$$\Delta I_{max} = \frac{R_i P_i \sqrt{2}}{V_g} \tag{10}$$

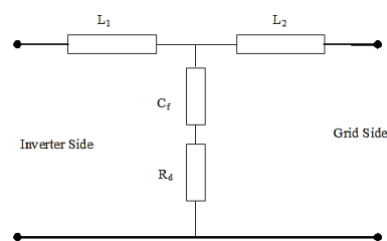


Fig. 4. LCL Filter

Step 4: Find inverter side impedance L_1

For designing the converter side inductance L_1 , the ripple content in the output current needs to be taken care of. Hence from [21] if ΔI_{max} is peak to peak ripple current of the filter output then L_1 is given Eq. (11). Where $T_s = 1/f_s$.

$$L_1 = \frac{V_{dc} T_{sw}}{8 \Delta I_{max}} \quad (11)$$

Step 5: The LCL filter has two resonance frequencies. The parallel resonance frequency is given by Eq. (12) and the series resonance frequency is given by Eq. (13)

$$\omega_p = \frac{1}{\sqrt{L_2 C_f}} \quad (12)$$

$$\omega_r = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \quad (13)$$

During series resonance the current will be maximum, hence the literature suggests that the series resonance of the LCL filter must be kept well above the fundamental frequency. To find the suitable resonance frequency, the series resonance ω_r is taken as $\omega_r = n \omega_g$ where $n > 10$.

Step 6: Find filter capacitor C_f , Let $L_1=L_2$

$$C_f = \frac{2}{\omega_r^2 L_1} \quad (14)$$

Step 7: Find damping resistor

$$R_d = \frac{1}{3 \omega_r C_f} \quad (15)$$

4. Simulation Results

Table 2 shows the parameters used for the simulation of the proposed inverters. LCL filter presented in the previous session is used to find the filter parameters. Along with leakage current and harmonic content, power flow management and power quality must be prioritised for optimal use of energy harvested and converted in a distributed power generation system [22]. Hence, a current control technique using a Direct-Quadrature frame with a PI controller is implemented for controlling active and reactive power [23]. MATLAB Simulink is used for the simulation of the topologies shown in Fig. 1 and Fig. 2 i.e, HB-ZVR inverters and proposed inverters. Fig. 5 shows the grid voltage and currents, common mode and differential mode characteristics

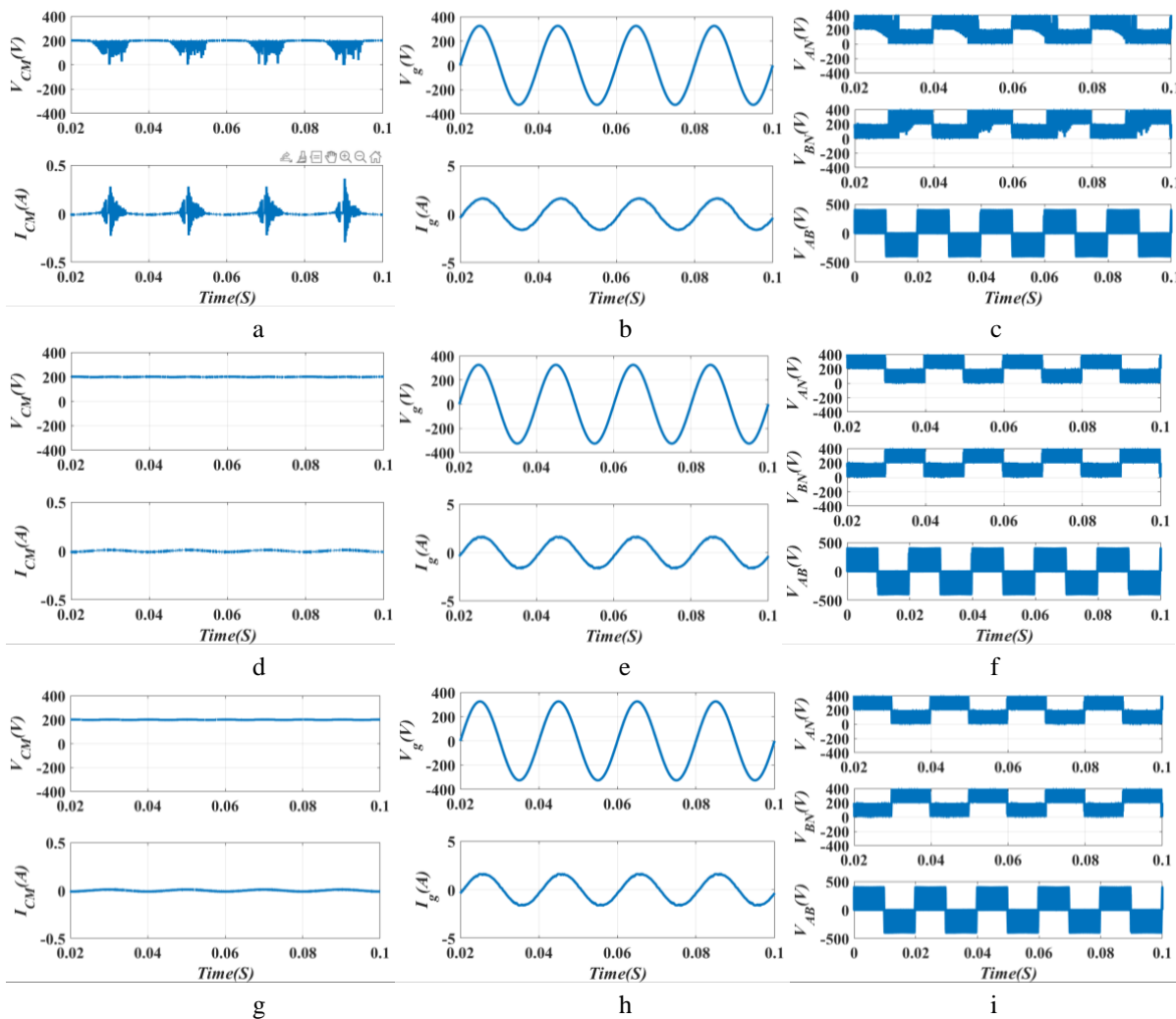


Fig. 5. HB-ZVR a. Common mode voltage and current b. Grid voltage and current c. Differential mode voltages HB-ZVRD d. Common mode voltage and current e. Grid voltage and current f. Differential mode voltages HB-ZVRS g. Common mode voltage and current h. Grid voltage and current i. Differential mode voltages

Table 2. Simulation Parameters

Power rating	P_i	1 kW
Grid voltage	V_g	230 V
Grid Frequency	f_g	50 Hz
Switching frequency	f_s	20 kHz
PV Voltage	V_{PV}	400 V
Split capacitor	C_1, C_2	560 μ f
Filter inductors	L_1, L_g	4 mH, 4 mH
Filter Capacitor	C_f	1 μ f
Parasitic Capacitor	C_{PV1}, C_{PV2}	0.1 μ f
MOSFET		SCT2750NY
Diode		C3D04060A

of HB-ZVR inverters. Similarly, Fig. 6 shows grid voltage and currents, common mode and differential mode characteristics of proposed inverters i.e, H5-ZVR, H5-ZVRD and H5-ZVRS. The common-mode leakage current statistical analysis of the inverters is listed in Table. 3. It can be observed that, compared to the conventional HB-ZVR, HB-ZVRD and HB-ZVRS topologies the proposed H5-ZVR and its derivatives are having less leakage current. The total harmonic distortion

of the inverters is 1.82%, 0.92%, 0.93% for HB-ZVR, HB-ZVRD and HB-ZVRS respectively. Similarly, total harmonic distortion of H5-ZVR, H5-ZVRD and H5-ZVRS is 1.03%, 0.91% and 0.91% respectively. The rms and p-p value of leakage current must be within 30mA and 300 mA respectively [24-25] and current harmonics distortion allowed is less than 5% as per [26-27]. This shows that the proposed H5-ZVR and its derivatives again outperform compared to HB-ZVR topologies and also the parameters are within acceptable limits as per the standards. Table. 3 also lists a comparison of proposed topologies with the conventional inverters. All the parameters listed in the table are obtained by simulating the topologies with the simulation parameters given in Table.3 to check the validity of the output. Table.3 also lists the calculated efficiency of the proposed inverters. Fig.7 shows the plot of efficiency at varying loads. The calculations are performed using the analysis presented in [33]. The graph shows that the efficiency of the proposed inverter is slightly lesser than the reference topologies due to the inclusion of an extra switch for DC decoupling. However, the common mode characteristics of the proposed inverters supersede the basic full-bridge ZVR topologies.

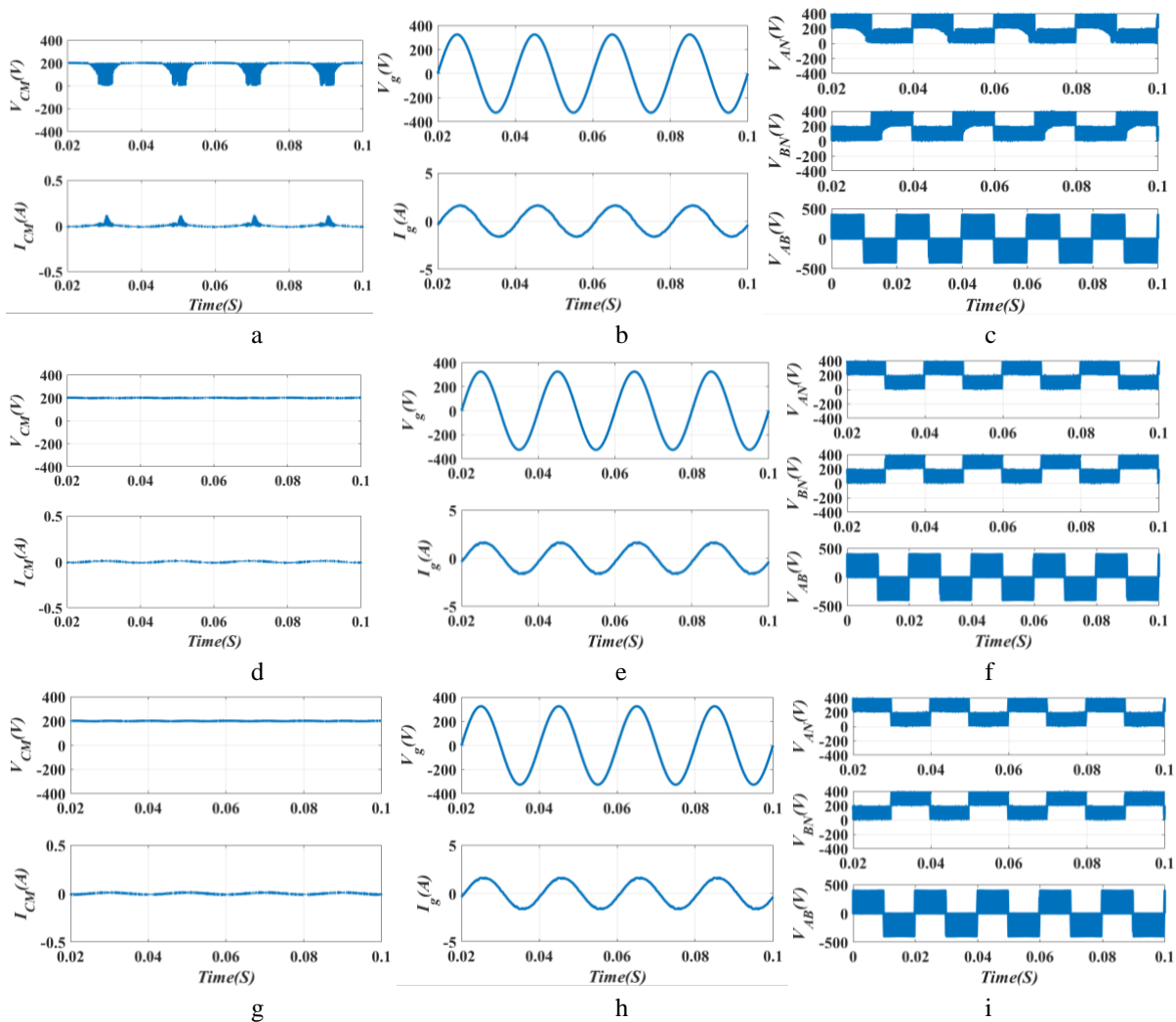


Fig. 6. H5-ZVR a. Common mode voltage and current b. Grid voltage and current c. Differential mode voltages H5-ZVRD d. Common mode voltage and current e. Grid voltage and current f. Differential mode voltages H5-ZVRS g. Common mode voltage and current h. Grid voltage and current i. Differential mode voltages

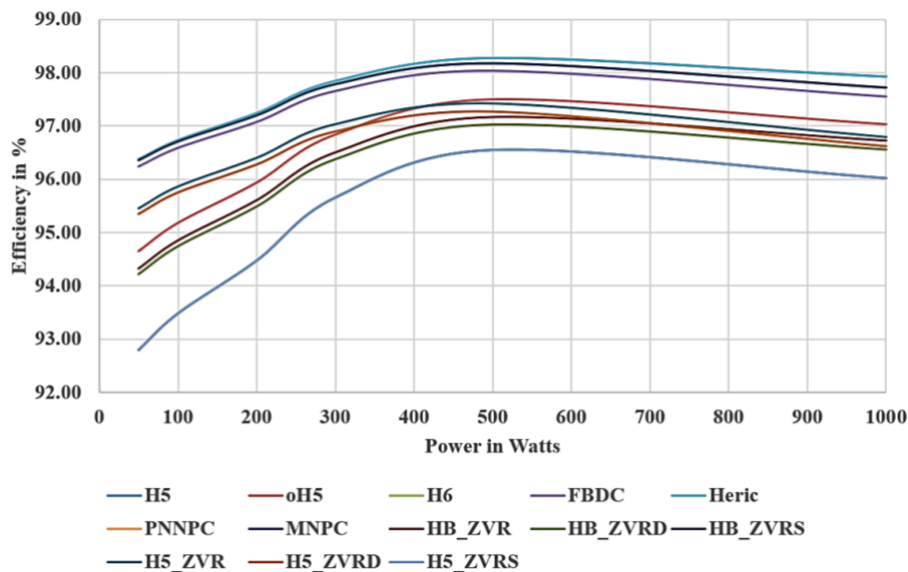


Fig. 7. Efficiency of inverter at different load

Table.3. Comparisons of inverter topologies

	No. of Switch	No. of Diode	Leakage current mA p-p	Leakage Current mA rms	Common mode Voltage	Efficiency %
H5[15]	5	0	282	15.3	0 to V_{pv}	NA
oH5[28]	6	0	281	14.5	$V_{pv}/4$ to $V_{pv}/2$	NA
Heric[16]	6	0	275	14.7	0- V_{pv}	NA
H6[29]	6	0	294	15.5	0- $V_{pv}/2$	96.3
FBDC[30]	6	2	50	7.5	0- $V_{pv}/2$	97.4
FBDC (2fs)[7]	6	2	66	9.3	0 - V_{pv}	NA
PNNPC [31]	8	0	68	8.19	0	96.53
MNPC [32]	7	2	47	7.5	0	97.28
HB-ZVR [18]	5	4	644	35	0- $V_{pv}/2$	95.25
HB-ZVRD	5	6	24	7.281	0	96.25
HB-ZVRS	6	4	675	23	0	96.28
H5-ZVR	5	4	135	10	0- $V_{pv}/2$	96.96
H5-ZVRD	5	6	31	7.3	0	96.82
H5-ZVRS	6	4	30	7.3	0	95.21

5. Conclusion

This paper presents a novel H5-ZVR, H5-ZVRD and H5-ZVRS topologies which are derived by integrating H5 topology with the HB-ZVR and its derivative topologies. In the paper, an effort is made to combine the two leakage current reduction techniques i.e., AC-bypass and DC-bypass and it is observed that it is possible to improve the performance of the inverter by adopting more than one in a single inverter. The topologies are simulated and compared with the existing traditional topologies and it is observed that by this method it is possible to reduce the leakage current and can improve differential mode characteristics as well. In the paper only H5 topology is taken into consideration for the trial purpose, the same thing can be experimented with other DC bypass techniques to arrive at new improved topologies.

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