Using Parallel Capacitor-based BFCL with MOV for Enhancing the LVRT Performance of SEIG-Based Wind Power Plants

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Abstract- The capability of Low-voltage ride-through (LVRT) is core of grid code requirements for integration of wind power plants (WPPs) to power system. This study proposes a parallel capacitor-based bridge-type fault current limiter (PCBFCL) with metal oxide visitor (MOV) to comply the LVRT requirement of WPPs. The configuration of conventional parallel capacitor-based BFCL in two steps is modified and developed to comply the WPP LVRT requirements. Extended time domain simulations are carried out in PSCAD/EMTDC environment to prove the efficiency of the PCBFCL under symmetrical and unsymmetrical faults. Also, its capability is compared with the series dynamic resistor (SDR). The WPP model is based on equivalent aggregated self-excited induction generator (SEIG). Simulation results show that, the PCBFCL provides the most effective series device to satisfy the LVRT capability of SEIG-based WPPs and has superior performance compared with the SDR.

Keywords: Wind Power Plants (WPP), Low-Voltage Ride-Through (LVRT), Parallel Capacitor-based Bridge-type Fault Current Limiter (PCBFCL), Self-Excited Induction Generator (SEIG), Reactive Power

1. Introduction

Owing to increasing the impact of wind power plants (WPPs) on power system operation, system operators have been modified their grid code requirements (GCRs) to ensure the stability of power system [1]. One of these, is the LVRT requirement [1-2]. Considering Fig. 1(a), the WPPs should remain connected under voltage sag condition based on voltage-time profile. Furthermore, they have to provide reactive power to help the terminal voltage during and after fault as presented in Fig. 1(b). Among wind turbine (WT) technologies employed in WPPs, the variable speed-bases WTs with doubly-fed induction generator (DFIG) is attractive due to capability of power flow control, maximum power tracking in variable speeds and high efficacy [3-4]. However, there are many fixed speed WTs with self-excited induction generator (SEIG) which is employed from last years in WPPs [5-6]. They have inexpensive, robust and simple structure. However, they cannot satisfy the LVRT requirement alone and need external devices [2-3]. In literature, several external devices have been employed to cope with this problem, which can be classified as: 1) shunt flexible AC transmission lines (FACTs) controllers include STATCOM and SVC [7-8],2) custom power devices such as dynamic voltage restorer (DVR) [9-10] and unified power quality conditioner (UPQC) [11], 3) series FACTs controllers include unifies inter-phase power controller (UIPC) [12-13], static synchronous series compensator(SSSC)[14], 4) series dynamic resistor (SDR) [15-16],

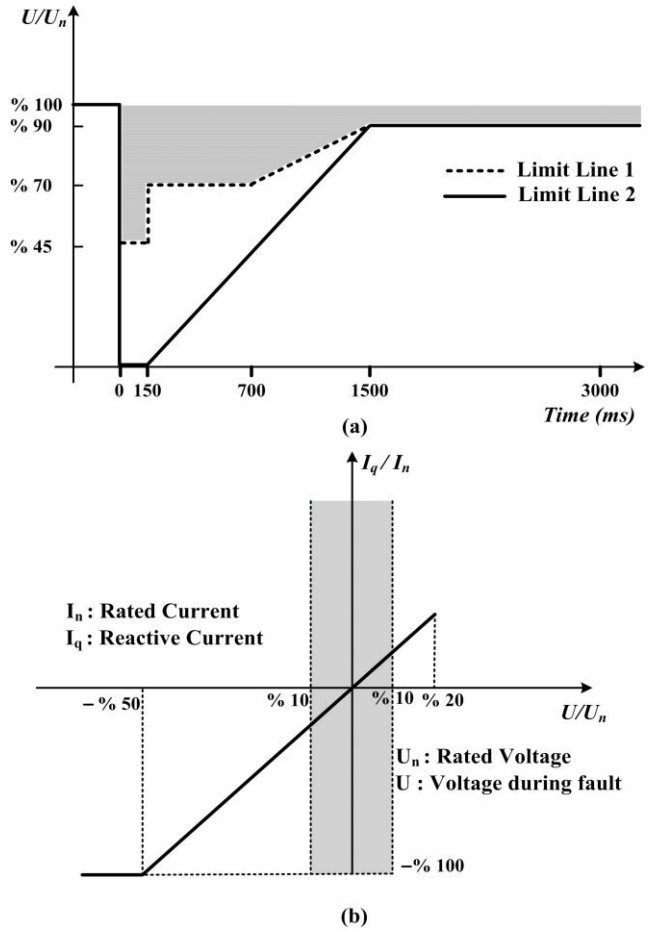


Fig. 1. LVRT requirement of E.ON grid code, (a) voltage limit profile, (b) injected reactive current profile

5) energy storage system (ESS) [17], 6) pitch angle control (PAC) [18], 7) fault current limiters (FCLs) [19-31]. Application of shunt FACTs controllers provide the reactive current after fault clearance to meet the reactive current LVRT requirement [7-8].

The application of DVR, UIPC, SMES, SSSC and UPQC offers a most effective series interface to satisfy the LVRT, however, they require high capacity and high cost power converters, which make these devices infeasible for LVRT performance enhancement [32-33]. The speed change of pitch angle is relatively slow, which limits the performance of PAC to meet the LVRT requirement [34]. Among these devices, the application of FCLs includes superconducting FCLs (SFCLs), [19-23] and solid-state FCLs (SSFCLs) [24-32] were recognized as effective solution. In [19-21], resistive-type SFCL have been used for grid connection WPPs to enhance transient stability. In [22] and [23], application of bridge-type and sutured-type SFCLs have been used for enhancing the LVRT capability of WPPs, respectively. Application of the SFCLs offers a reliable and feasible series interface for connecting WPPs to grid, however, this solution is very expensive due to require cooling system and superconducting material. In [24], the using of bridge-type FCL (BFCL) based on the DC reactor was suggested to improve the LVRT capability and was compared with the SDR. In [24], it is stated that the BFCL is better than the SDR. Also, this type of BFCL was used for power quality and transient stability enhancement in [25-27]. In [28], the BFCL with different configuration from the one used in [24] has been proposed, which an inductor was used in parallel with BFCL as limiting impedance. In [29], a resistor has been used connected instead of inductor to increase the LVRT capability. In [30-31], limiting impedance includes a series inductor and resistor has been used to improve the LVRT capability. Although, the application of both BFCLs in different configuration effectively enhances the LVRT, however, they cannot provide reactive power to meet the reactive current LVRT requirement. Because of this, additional reactive power compensator scheme like STATCOM is necessary to meet this requirement. In [35], a distribution static compensator (DSTATCOM) together with a BFCL is applied in parallel and series with the wind generator to enhance the LVRT capability, respectively.

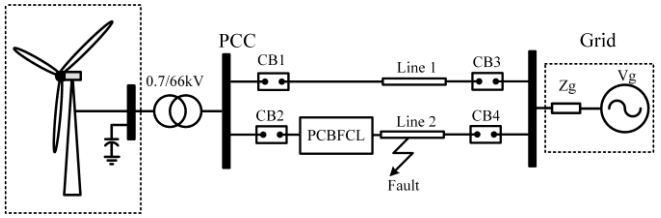
The discharging resistor of the BFCL dissipates the output active power of the wind generator and prevents rotor acceleration during fault. Also, The DSTATCOM injects the reactive current to help the terminal voltage in compliance with the LVRT requirement. The application of the BFCL together with the DSTATCOM effectively complies the LVRT requirement of WPPs, however, it will impose high cost of DSTATCOM implementation. In [36], a parallel capacitor and a limiting resistor has been used in AC and DC side of the BFCL circuit, respectively. The parallel capacitor provides reactive power needed of WPPs and the limiting resistor dissipates the DFIG active power to fulfil the LVRT requirements of WPPs under fault conditions. However, the parallel capacitor produces high transient spike over-voltage during fault due to step change of voltage drop across of the BFCL circuit at IGBT switching times. Also, it requires high current rating diodes to carry the fault current due to insertion of the limiting resistor in DC side of BFCL.

This paper proposes the parallel capacitor BFCL (PCBFCL) to overcome the BFCL problems and provide both capabilities of DSTATCOM/BFCL to satisfy the LVRT requirements of self-excited induction generator (SEIG)-based WPP environments. To achieve this, a metal oxide varistor (MOV) is used in parallel with the parallel capacitor to protect the BFCL against transient over-voltage during fault due to step change of voltage drop across of the BFCL circuit. Also, the limiting resistor of the BFCL is placed in the AC side in parallel with the capacitor, which reduces the diodes current ratings. The efficiency of the PCBFCL is proved through time domain simulation and performance

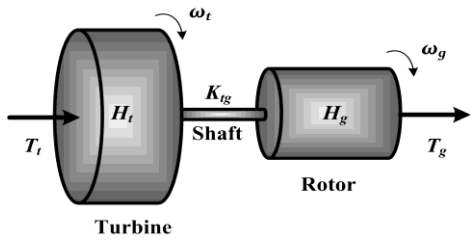
comparison of the SDR under symmetrical and unsymmetrical faults. Simulation studies have been performed in PSCAD/EMTDC software environment

2. Description of the WPP Model

In this study, an aggregated 20 MW SEIG-based WPP has been simulated in PSCAD/EMTDC environment. It is depicted in Fig. 2(a). The grid is modelled by a voltage source (V_g) in series with impedance (Z_g). The WPP is integrated to the grid by double circuit transmission lines (line 1 and line 2). Symmetrical as well as asymmetrical faults were applied at line 2 to evaluate capability of the proposed PCBFCL. The PCBFCL is located in series with faulted line (*i.e. Line 2*). The simulated system and internal SEIG parameters are presented in Table1.The WT, SEIG and drive train system are three main components of WPPs, which are modelled as follows:



(a)



(b)

Fig. 2. (a) Test system with SEIG-based WPP and PCBFCL, (b) Drive train system

2.1. Wind Turbine

The MOD2 wind turbine model of the PSCAD/EMTDC master library is used in this study. The mechanical power (P_m) obtained from the conversion of wind energy through the WT can be presented, as follows [37]:

$$P_m=0.5\pi\rho C_p(\lambda,\beta)R^2 V_W^3 \quad (1)$$

where in (1), V_w = wind speed, ρ = Air density, R = radius of blades and, C_P represents the power coefficient, which is a function of the λ and β. They represent the tip speed ratio and pitch angle, respectively.

2.2. SEIG Model

In this study the seven-order model induction generator in a *d-q* reference frame, which provided in the master library of PSCAD/EMTDC software is utilized [38].

Table 1. Wind Generator and grid parameters

	Parameters	Value
Grid	Rated voltage	33 kV
	Grid Frequency	50Hz
	X_g/R_g ratio	5
Induction Generator	Rated Active power	2MW
	Rated voltage	690V
	Rated frequency	50 Hz
	Inertia constant	1s
	Stator resistance	0. 0057 Ω
	Stator leakage reactance	0.078 Ω
	Rotor resistance	0. 0159 Ω
	Rotor leakage reactance	0.1022 Ω
	Mutual reactance	2.434 Ω
PCBFCL	DC reactor inductance	0.01 H
	C_{sh}	50uF
	R_D	20 Ω

2.3. Wind Turbine Shaft Model

The two-mass model is used for the LVRT performance study, in this work [37]. Fig. 2(b) shows the two-mass model, which composed of three main components include as follow:

- Blades with hub, which is presented as inertia H_t,
- The coupled rotor shaft and turbine is represented with K_{tg}
- Rotor and Gearbox, which is presented by H_g.

The two-mass drive train model is defined by below equations:

$$\begin{bmatrix}\dot{\omega}_g\\ \dot{\omega}_t\\ \dot{\delta}_{tg}\end{bmatrix}=\begin{bmatrix}\frac{D_{tg}}{2H_g} & \frac{-D_{tg}}{2H_g} & \frac{K_{tg}}{2H_g}\\ \frac{D_{tg}}{2H_t} & \frac{-D_{tg}}{2H_t} & \frac{-K_{tg}}{2H_t}\\ -1 & 1 & 0\end{bmatrix}\begin{bmatrix}\omega_g\\ \omega_t\\ \delta_{tg}\end{bmatrix}+$$

$$\begin{bmatrix}\frac{-1}{2H_g} & 0 & 0\\ 0 & \frac{1}{2H_t} & 0\\ 0 & 0 & 0\end{bmatrix}\begin{bmatrix}T_g\\ T_t\\ 0\end{bmatrix} \quad (2)$$

2.4. SEIG under Fault

The voltage and flux equations of the induction generator in the synchronous reference frame are expressed as [38]:

$$V_s = r_s i_s - L_s \frac{di_s}{dt} + L_m \frac{di_r}{dt} + j\omega_s \psi_s \quad (3)$$

$$V_r = r_r i_r - L_r \frac{di_r}{dt} + L_m \frac{di_s}{dt} + j(\omega_s - \omega_r)\psi_r \quad (4)$$

$$\psi_s = r_s i_s + L_m i_r \quad (5)$$

$$\psi_r = r_s i_r + L_m i_s \quad (6)$$

Here, L_s and L_r present the stator and rotor leakage inductances, respectively. Also, L_m presents the magnetizing inductance. R_r and R_s present the rotor and stator resistance, respectively. i_s and i_r are the current flow of the stator and rotor circuits, respectively. ω_r and ω_s present the rotor and stator angular frequencies, respectively. By neglecting the resistance of stator and rotor circuits, we have:

$$\frac{L_m}{L_s} V_s = -\sigma \frac{di_r}{dt} - j\sigma L_r(\omega_s - \omega_r) i_r + j\omega_r \frac{L_m}{L_s} + V_r \quad (7)$$

where, σ is the leakage coefficient and is defined by $\sigma = 1-(L_m^2/L_sL_r)$. In SEIGs, the rotor circuit is short circuit. Thus, a sudden change in the stator voltage results in the following equation:

$$\frac{L_m}{L_s} \Delta V_s = -\sigma \frac{di_r}{dt} \quad (8)$$

Equation (8) states that, the rotor current change magnitude depends on the stator voltage sag depth at fault inception instant. Therefore, voltage sag decline can reduce the transient magnitude rotor and stator current.

3. Principle Operation of the PCBFCL

Fig. 3(a) presents the BFCL power circuit presented in [36] to improve the LVRT performance of the DFIG-based WPP. The performance of this BFCL has two main problems under operation during fault.

- It requires high current rating diodes to carry the fault current due to being on the DC side of the BFCL.
- The C_{sh} produces high transient spike overvoltage across of the BFCL circuit at the IGBT switching times as shown in Fig. 3 in scenario A, which can cause failure operation of the BFCL.

In this paper, it is modified in two steps to cope with the aforementioned problems of operation during fault as demonstrated in Fig. 3(b). At first, the limiting resistor of the BFCL is placed in the AC side in parallel with the C_{sh}. By applying this change, only the normal current flows through the diodes, which leads to lower current rating diodes and voltage stress across of semiconductor switches under fault condition. Also, in the second step, a MOV is used in parallel with the RC circuit to protect the BFCL against transient over-voltage [39], at switching fault instants as demonstrated in Fig. 4. The V_K and V_P represent the protected level of the MOV and the peak value of transient over voltage across of the BFCL power circuit.

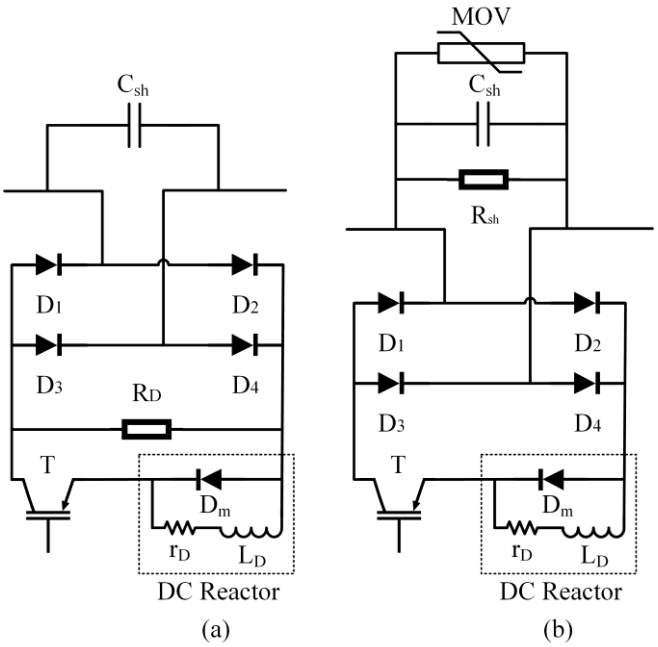


Fig. 3. (a) BFCL power circuit reported in [36] and (b) PCBFCL power circuit

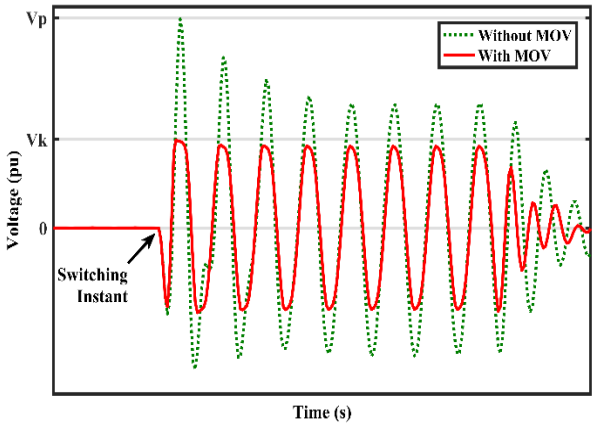


Fig. 4. Voltage across on the PCBGFCL with and without PCBFCL

3.1. Configuration of PCBFCL

The power circuit of the PCBFCL is illustrated in Fig. 3(a). It is composed of following parts:

- A diode bridge rectifier comprising D_1-D_4 to convert the AC current to DC current
- A DC reactor (L_D) to prevent high *di/dt* on the IGBT switch and decrees the rate of increasing fault current at fault inception time
- An Insulated-gate bipolar transistor (IGBT) semiconductor switch (T), which connected in series with the L_D
- A freewheeling diode (D_m) in parallel with the L_D
- A discharging resistor (R_{sh}) to mitigate the output power from SEIG during fault, and

- Parallel AC capacitor (C_{sh}), which incorporated with the bridge circuit to compensate the needed reactive power during and after fault,
- A MOV to protect the PCBFCL against transient over-voltage at fault inception time.

3.2. PCBFCL Operation and Control

In normal steady state operation mode, the T is close. The following current through line (i_L) is converted to DC current (i_d) by diode bridge rectifier circuit and flows through D_4-L_D-T - D_4 path for positive half cycle and D_2-L_d-D_3-T path for negative half cycle. In this state the DC reactor acts like a short circuit and offers low impedance path. Due to large impedance paths of the C_{sh} and R_D, current will flow from these paths, approximately. The voltage drop in this state is due to the r_d and forward voltage of D_1-D_4 and T, which are ignorable. The r_d represents the resistance of DC reactor. When a fault occurs, the i_d starts to rise suddenly, however, the L_D impeded from sudden change of the i_d and subsequently i_L. At the same time, the large inrush current attempts to flow through the C_{sh} caused by step change voltage across of the C_{sh}, which is limited by MOV and prevent from failure operation. Also, the T is protected from di/dt at fault inception time. At the time i_d increases to the threshold current (i_{d_ref}), the PCBFCL control circuit opens the T. After, turning off the T, the R_D and C_{sh} is inserted in the line current path and the DC reactor stored energy is freewheeled through the D_m. Further limiting the short circuit current, the R_D consumes the SEIG active power and the C_{sh} generates the reactive current demand to support the voltage of PCC in compliance with the reactive current LVRT requirement. After fault clearance, the system begins to return the pre-fault condition and the control system closes the T and the PCBFCL operation returns back to the steady-state operation mode.

3.3. PCBFCL Control System

Fig. 5 (a) presents the block diagram of the PCBFCL control system. The PCC voltage (V_{PCC}) and DC reactor current (i_d) are used to produce the T gate control signal. It includes two comparators include COM1 and COM2. The COM1 compares the i_d with the reference value (i_{d_ref}) and when $i_d \leq i_{d\_ref}$, the output of COM1 goes on low. The COM2 compares the V_{PCC} with the reference value (V_{PCC_ref}) and when $V_{PCC} \geq V_{PCC\_ref}$, the output of COM2 goes on high. In normal steady state operation mode, the V_{PCC} is higher than V_{PCC_ref} and the i_d is lower than i_{d_ref}. therefore the output of both comparators go on high and considering logical control, the pulse generation part of the controller provides high voltage gate signal (VGS) to close the T. when a fault occurs, the V_{PCC} drops and the i_d starts to increase. Therefore, the i_d will higher than the i_{d_ref} (*i.e* .$i_d \geq i_{d\_ref}$) and the V_{PCC} will lower than the V_{PCC_ref} (*i.e.* $V_{PCC} \leq V_{PCC\_ref}$). for this condition both comparators become low and controller provides low VGS to open the T. After fault clearance, the PCC voltage is restored to pre-fault value and the V_{PCC} will higher than the V_{PCC_ref}. however, the i_d remains higher than i_{d_ref}. Therefore, the output of COM1 changes to low level, however, the output of the COM2 remains in high level. In this condition the controller close the T again. The flowchart the PBFCL performance is presented in Fig. 5(b).

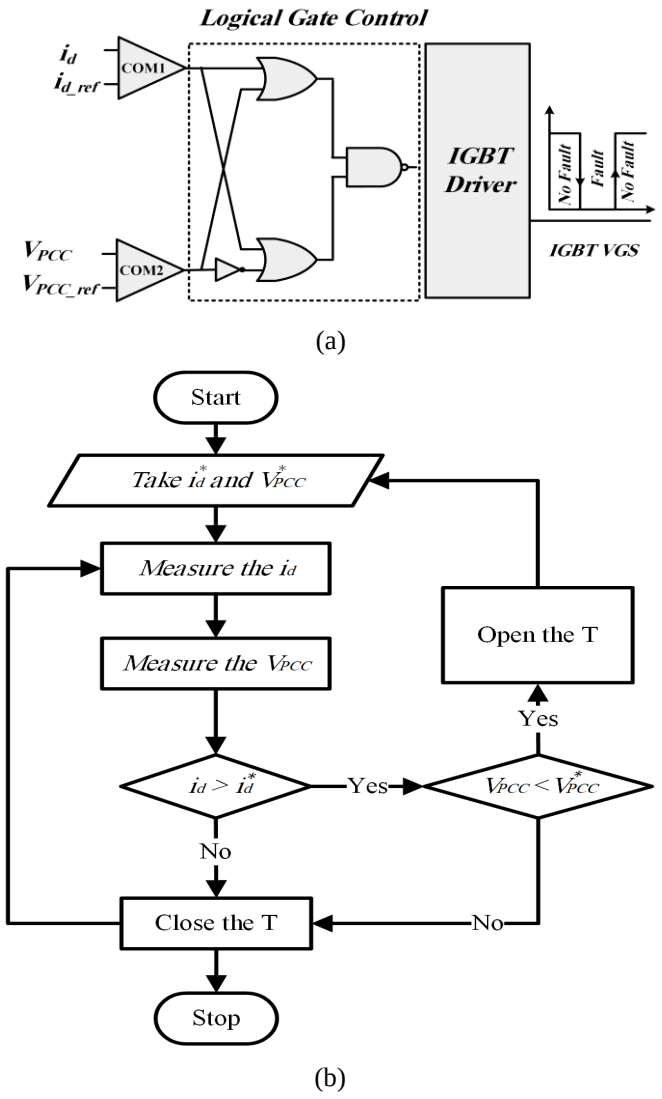


Fig. 5. (a) Control system of the PCBFCL, and (b) Flowchart of the PCBFCL performance

4. SDR Operation

In this work a comparative study between the PCBFCL and SDR is performed to investigate the effectiveness of the PCBFCL in terms of the LVRT capability. The SDR is a proved LVRT enhanced scheme, comprising a bypass power electronic based switch in parallel with a pre-insertion resistor (R_D) [15-16]. The voltage of PCC bus (V_{PCC}) is measured as control signal of the SDR operation. In normal steady state operation mode, the V_{PCC} is higher than $V_{PCC\_ref.}$ and the R_D is bypassed. When a fault occurs, the V_{PCC} drops below the $V_{PCC\_ref.}$ and the control system opens the bypass and inserts the R_D in series with faulted line and thus increases the PCC that, the reactive power absorbed from grid reaches to 2.5 pu, when no auxiliary scheme is used, which could lead to the system voltage instability. However,

by using the PCBFCL and SDR, the reactive power absorbed from grid is effectively reduced and the PCBFCL offers lower absorption reactive power from grid. Fig 8 (c) presents the reactive power flow from line 1 for all scenarios. It is seen that, by using the PCBFCL scheme, 1.5 pu reactive power injected to grid through line 1, which provides the lowest voltage sag at the PCC bus in this scenario. Also, Fig 8 (d) presents the reactive power flow from faulted feeder, which the SDR and PCBFCL has been located. It is seen that, the PCBFCL generates reactive current to help the grid voltage stability in compliance with the LVRT requirement.

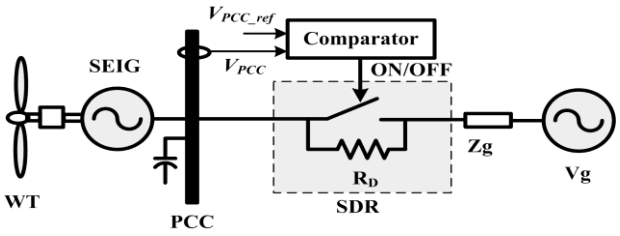


Fig. 6. Schematic diagram of the SDR connected to WPP

voltage and dissipates the output active power during the fault period. It is placed in the same location of the PCBFCL as shown in Fig. 1(a).

5. Simulation Results

PSCAD/EMTDC software has been used to conduct the simulations in this work. For LVRT analysis, both symmetrical three-line-to-ground (3LG) and unsymmetrical line-to-ground (SLG) short circuit faults are applied in line 2. Both 3LG and SLG short circuit faults are pre-set to occurs at *t=10s*. Fault duration and fault impedance are considered to be *150ms* and *1mΩ*, respectively. The wind speed is set fixed at W_w*=12m/s*. Three different scenarios are considered in the simulations; they are as follows:

- **Scenario A:** Without FCL
- **Scenario B:** With SDR
- **Scenario C:** With PCBFCL

5.1. LVRT performance Analysis for 3LG Fault

The performance of the PCBFCL under 3LG fault is shown in Fig.7 and 8. Fig 7(a) presents the fault current flowing from line 2. It can be seen that, the fault current raises to 4pu and 4.6 pu at the fault inception and clearing instants. However, by using the PCBFCL the fault current is effectively limited and it performs better than the SDR. Fig. 7(b) presents the SEIG rotor currents. As illustrated in this figure, the sudden jump in rotor current is limited at the fault inception time in scenario C. Fig. 7(c) presents the PCC voltage profile for all scenarios. For scenario A, the PCC voltage drops to zero. By using the PCBFCL and SDR, the PCC voltage sag is reduced. However, the PCBFCL performance is better than the SDR with lower voltage sag during fault period. Fig. 7(d) presents the SEIG rotor speed for all scenarios. The PCBFCL and SDR effectively limit the rate of rise of rotor speed. However, the PCBFCL gives lower oscillation compared with the SDR.

Fig. 8(a) presents the WPP active power for all scenarios. In scenario A, the WPP active power drops to almost zero. Using the PCBFCL and SDR keep the active power profile smooth during fault, however, the application of PCBFCL has lower oscillation and power drop compared with the SDR.

Fig. 8(b) presents the WPP reactive power for all scenarios. It is seen that, the reactive power absorbed from grid reaches to 2.5 pu, when no auxiliary scheme is used, which could lead to the system voltage instability. However, by using the PCBFCL and SDR, the reactive power absorbed from grid is effectively reduced and the PCBFCL offers lower absorption reactive power from grid. Fig 8 (c) presents the reactive power flow from line 1 for all scenarios. It is seen that, by using the PCBFCL scheme, 1.5 pu reactive power injected to grid through line 1, which provides the lowest voltage sag at the PCC bus in this scenario. Also, Fig 8 (d) presents the reactive power flow from faulted feeder, which the SDR and PCBFCL has been located. It is seen that, the PCBFCL generates reactive current to help the grid voltage stability in compliance with the LVRT requirement.

5.2. LVRT Performance Analysis under SLG Fault

Fig. 9 presents the simulation results under SLG fault condition. Fig. 9(a) represents the fault current flowing through the faulted line for all scenarios. For scenario A, the fault current raises to 2.8 pu and 2 pu at the fault inception and clearing instants, respectively. By using the PCBFCL, the fault current is limited like in the case of using the SDR. As shown Fig. 9(b), the transient rotor current is significantly limited at the fault inception and clearing instants in both scenarios B and C. Fig. 9(c) represents the PCC voltage profile under SLG fault condition. In the scenario A, the PCC voltage reduces to 0.7 pu. The PCC voltage drop is effectively decreased by using both PCBFCL and SDR. However, the PCBFCL has superior performance compared with the SDR in view point of lower voltage sag and faster voltage recovery. Fig. 9 (d) shows the rotor speed for SLG fault. It can be seen from this figure, the speed oscillation is lower in the case of using the PCBFCL, like the 3LG fault.

Fig. 10(a) shows the active power response subject to SLG fault for all scenarios. It is clear that the active power drop is the lowest during fault for the scenario C and the active power fluctuation is the lowest after fault clearance in the scenario B.

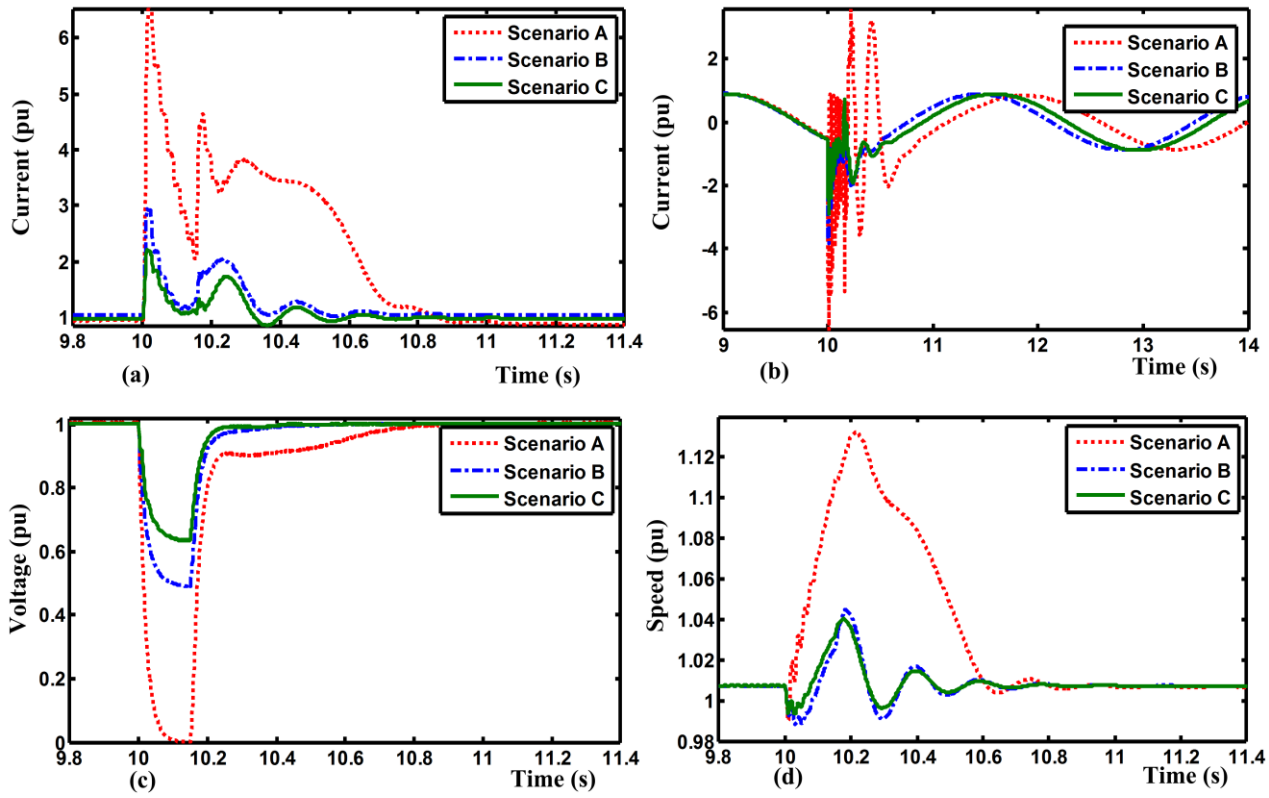


Fig. 7. WPP response for 3LG fault (a) fault current contribution of the WPP, (b) SIEG rotor current, (c) PCC voltage and, (d) rotor speed

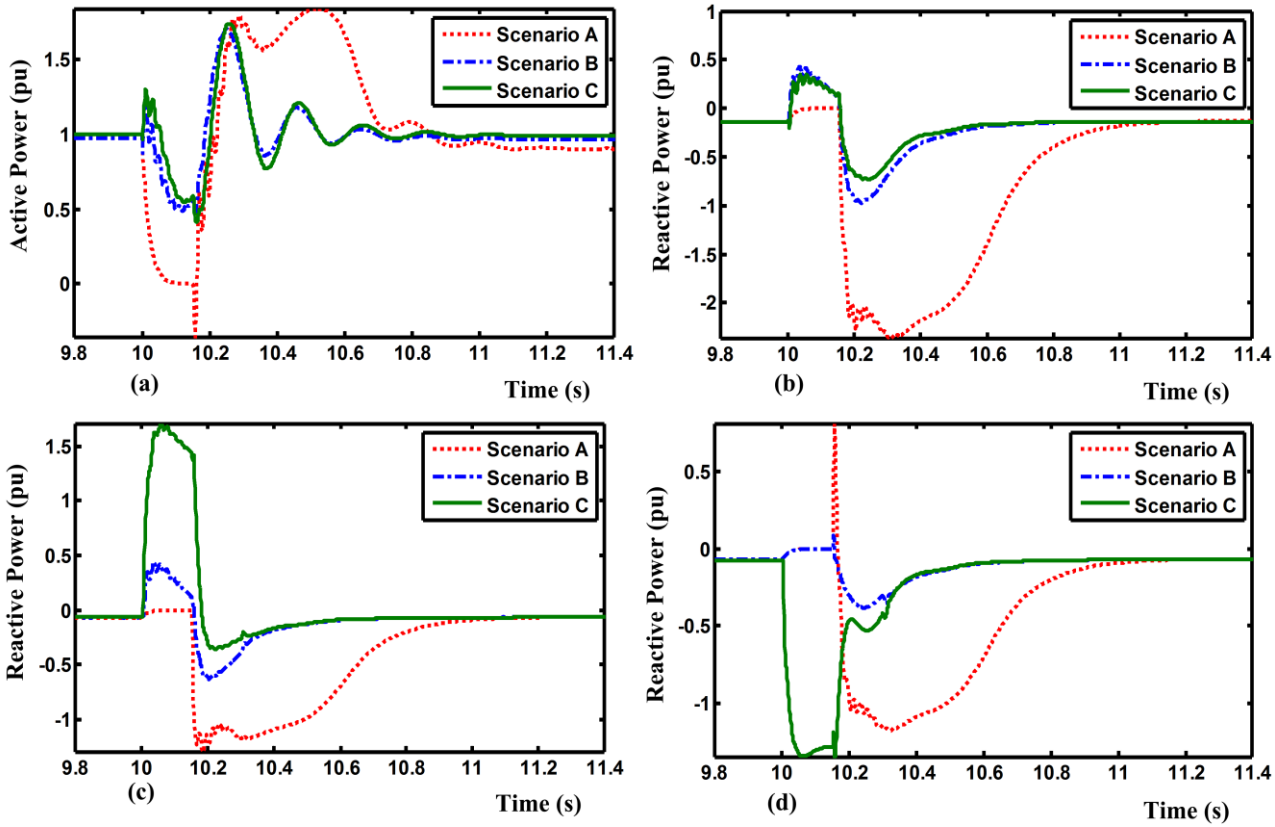


Fig. 8. WPP response for 3LG fault (a) output active power of the WPP, (b) reactive power of the WPP , (c) reactive power flow through line 1 and, (d) reactive power flow through line 2

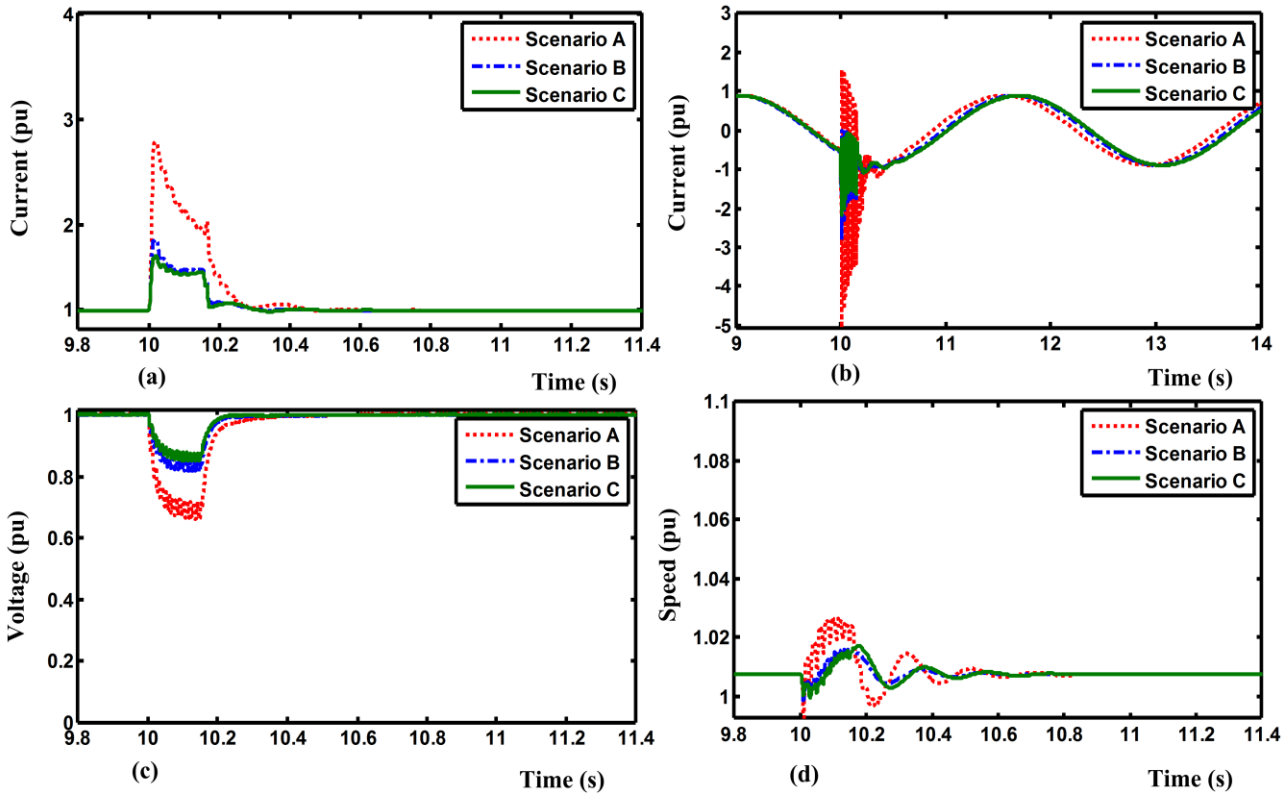


Fig. 9. WPP response for SLG fault (a) fault current contribution of the WPP, (b) SEIG rotor current, (c) PCC voltage, (d) rotor speed

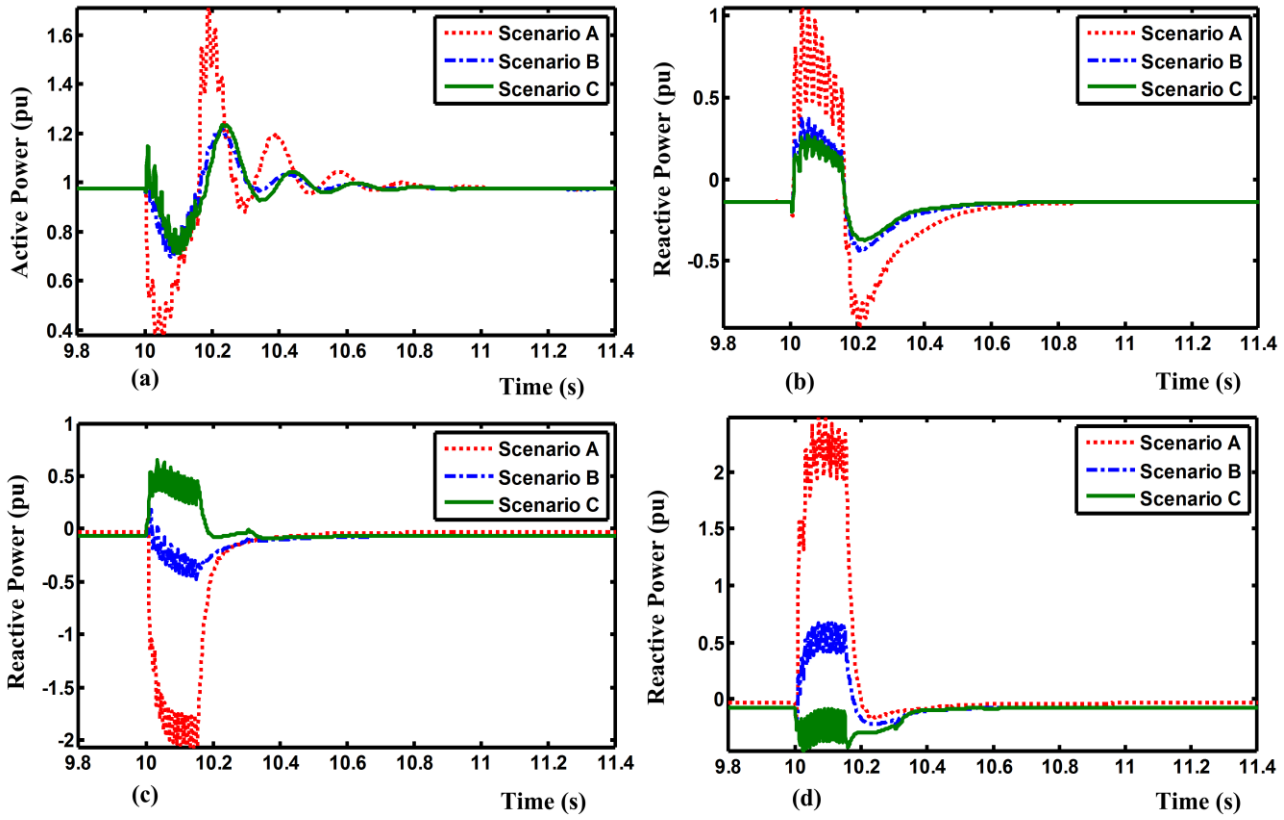


Fig. 10. WPP response for SLG fault (a) output active power of the WPP, (b) reactive power of the WPP, (c) reactive power flow through line 1 and, (d) reactive power flow through line2

As shown in Fig. 10 (b), the reactive power absorption by the WPP is lowest with the PCBFCL application during fault in the scenario C. Considering Fig. 10(c), the WPP consumes 2.05 pu and -0.35 reactive power through line 1 for scenarios A and B, respectively. However, in scenario C, the PCBFCL generates o.5 pu reactive power and injects to grid through line 1, which leads to the lowest PCC voltage sag in this scenario. Fig. 10(d) represents the faulted line (line 2) reactive power. Like 3LG fault, after fault clearance, in scenario C, the C_{sh} of the PCBFCL produces 0.5 pu reactive power to comply the LVRT requirements.

5.3. PCBFCL power circuit Operation under fault condition

In this section, the PCBFCL power circuit performance is compared with the BFCL performance presented in [36], under fault condition. Simulation are performed for two following scenarios:

- Scenario A: with the BFCL presented in [36]
- Scenario B: with the PCBFCL

Fig. 11 (a) presents the capacitor voltage for two scenarios. It can be seen that, the capacitor voltage in scenario A raises to 14kV at switching instant. However, by using the PCBFCL, the capacitor voltage is limited to 6kV. Fig. 11 (b) presents the capacitor current for two scenarios. It can be seen that, the capacitor current increases to 1.4 kA in scenario A. However, by using the PCBFCL, the capacitor current is limited in 0.7kA.

Fig. 12 (a) presents the bridge circuit current for two scenarios. It can be seen that, the bridge circuit current in scenario A increases to 1.4kA. However, by using the PCBFCL, no current flows through the bridge circuit. Fig. 12 (b) presents the current flow one of diodes for two scenarios. It can be seen that, the diode current increases to 1.4 kA in scenario A. However, by using the PCBFCL, no current flows it, which reduces the current rating of the diodes.

6. Conclusion

In this paper, the conventional BFCL has been developed and modified in three steps to adapt with WPP environment requirements. Also, the performance of the proposed PCBFCL is compared with the SDR under both symmetrical and asymmetrical faults. Based on simulation results, the following point can be drawn:

- The rating of the DC reactor is lower compared with the conventional BFCL. It allows the cost, weight, and volume of the DC reactor are reduced.
- The increment of the fault current and PCC voltage sag have been limited by DC reactor without any delay. It causes suppression of the transient rotor over currents at the both end of fault period.
- The parallel AC capacitor of the PCBFCL provides the needed reactive power of the WPP during fault, which satisfies the reactive current LVRT requirement of the SEIG-based WPP.

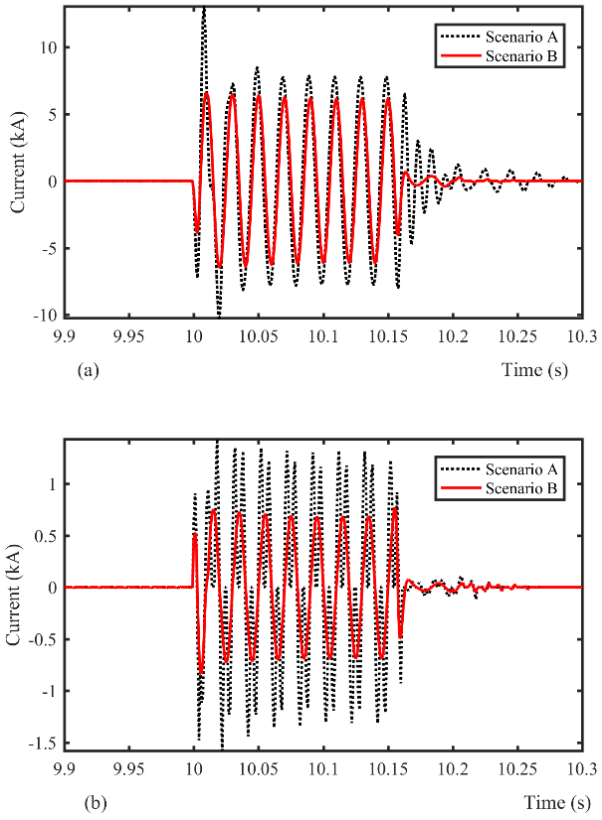


Fig. 11. (a) Capacitor voltage for two scenarios, (b) Capacitor current for two scenarios

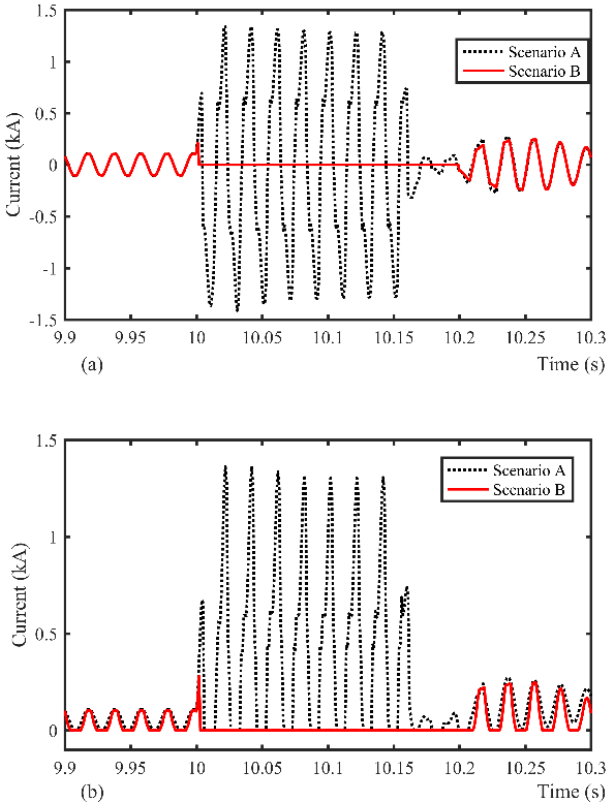


Fig. 12. (a) diode bridge rectifier for two scenarios, (b) diode current for two scenarios

- The discharging resistor of the PCBFCL dissipates excess output active power from the WPP during the fault period, which helps to the SEIG rotor speed stability.
- The PCBFCL shows better LVRT performance than the SDR.
- The MOV protect the PCBFCL from overvoltage under fault condition.
- The current rating of the PCBFCL diodes are effectively reduced.

References

[1] O. Kiymaz, T. Yavuz ,"Wind power electrical systems integration and technical and economic analysis of hybrid wind power plants," 2016 5th International Conference on Renewable Energy Research and Applications (ICRERA), Birmingham, pp. 158-163, 20-23 Nov. 2016.

[2] M. Tsili and S. Papathanassiou, "A Review of Grid Code Technical Requirements for Wind Farms," IET Renewable Power Generation, Vol. 3, No. 3, pp. 308–332, Sept. 2009.

[3] M. M. Moghimian, M. Radmehr, M. Firouzi, "Series Resonance Fault Current Limiter (SRFCL) with MOV for LVRT Enhancement in DFIG-Based Wind Farms," Electric Power Components and Systems, Vol. 47, No. 19-20, pp. 1814-1825, March 2020.

[4] Z. Rafiee, M. Rafiee, M. R. Aghamohammadi, " A New Control Strategy based on Reference Values Changing for Enhancing LVRT capability of DFIG in Wind Farm," International Journal of Renewable Energy Research (IJRER), Vol. 9, No. 4, pp. 1626-1637, December 2019.

[5] M. Firouzi, "A modified capacitive bridge-type fault current limiter (CBFCL) for LVRT performance enhancement of wind power plants," International Transactions on Electrical Energy System, Vol. 28 , No. 3, pp. 1-15, December 2017.

[6] A. Ameri, Y. Amara, C. Nichita, "Impact of Fault Ride-Through on Wind Turbines Systems Design ," 2018 7th IEEE International Conference on Renewable Energy Research and Applications (ICRERA), Paris, pp. 567-575, 14-17 Oct 2018.

[7] H. H. Doostabad, M. R. Khalghani, M. H. Khooban, " A novel control system design to improve FRT capability of fixed speed wind turbines using STATCOM in presence of voltage fault," International Journal Electrical and Power Energy System, Vol. 77, pp. 280–286, May 2016.

[8] J. Chhor, P. Tourou, C. Sourkounis, "Evaluation of state-based controlled STATCOM for DFIG-based WECS during voltage sags," 5th International Conference on Renewable Energy Research and Applications (ICRERA), Birmingham, pp. 463-471, 20-23 Nov. 2016.

[9] E. El Hawatt, M. S. Hamad, K. H. Ahmed, I. F. El Arabawy, "Low voltage ride-through capability enhancement of a DFIG wind turbine using a dynamic voltage restorer with Adaptive Fuzzy PI controller", International Conference on Renewable Energy Research and Applications (ICRERA), Madrid, pp. 1234-1239, 20-23 Oct. 2013.

[10] Kh. Goweily, M. Sh. El Moursi, M. Abdel-Rahman, M. A. L. Badr, "Voltage booster scheme for enhancing the fault ride-through of wind turbines", IET Power Electronics, Vol. 8, No. 10, pp. 1853-1863, September 2015.

[11] Ch. Wessels, F. Gebhardt, F.W. Fuchs," Fault ride-through of a DFIG wind turbine using a dynamic voltage restorer during symmetrical and asymmetrical grid faults," IEEE Transaction on Power Electronic, Vol. 26, No. 3, pp. 807–15, March 2011.

[12] M. Firouzi, G. B. Gharehpetian, B. Mozafari, " Power Flow Control and Short Circuit Current Limitation of Wind Farms Using Unified Inter-Phase Power Controller," IEEE Transaction on Power Delivery, Vol. 32, No. 1, pp. 62-71, Jun 2017.

[13] M. Firouzi, G. B. Gharehpetian, S. B. Mozafari, "Application of UIPC to improve power system stability and FRT capability of SCIG-based wind farms," IET Generation, Transmission & Distribution, Vol. 11, No. 9, pp. 2314-2322, July 2017.

[14] M. S El Moursi, K. Goweily, J. Kirtley and M. Abdel-Rahman, "Application of Series Voltage Boosting Schemes for Enhanced Fault Ride through Performance of Fixed Speed Wind Turbines," IEEE Transactions on Power Delivery, Vol. 29, No. 1, pp. 61–71, May 2014.

[15] A. E. Makrini, Y. E. Karkri, Y. Boukhriss, H. E. Markhi, H. E. Moussaoui, "LVRT control strategy of DFIG based wind turbines combining passive and active protection", International Journal of Renewable Energy Research (IJRER), Vol. 7, No. 3, pp. 1626-1637, March 2017.

[16] K. E. Okedu, S. M. Muyeen, R. Takahashi, and J. Tamura, "Wind farm fault ride through using DFIG with new protection scheme," IEEE Transaction on Sustainable Energy, Vol. 3, No. 2, pp. 242–254, April 2012.

[17] S. T. Kim, B. K. Kang, S.H. Bae, J. W. Park, "Application of SMES and Grid Code Compliance to Wind/Photovoltaic Generation System," IEEE Transactions on Applied Superconductivity, Vol. 23, No. 3, June 2013.

[18] A. Muneer, M. B. Kadri , "Pitch angle control of DFIG using self-tuning neuro fuzzy controller", International Conference on Renewable Energy Research and Applications (ICRERA), Madrid, pp. 316-320, 20-23 Oct. 2013.

[19] P. M. Tripathi, S. S. Sahoo, K. Chatterjee, "Enhancement of low-voltage ride through of wind energy conversion system using superconducting saturated core fault current limiter," International Transactions on Electrical Energy Systems, Vol. 29 , No. 4, pp. 1-19, April 2019.

[20] M. S. El-Moursi, "Fault ride through capability enhancement for self-excited induction generator-based wind parks by installing fault current limiters," IET Renewable Power Generation, Vol. 5. No. 4, pp. 269–280, July 2011

[21] A. Heidary, H. Radmanesh, K. Rouzbehi, and H. Moradi CheshmehBeigi, "A Multifunction High-Temperature Superconductive Power Flow Controller and Fault Current Limiter," in IEEE Transactions on Applied Superconductivity, Vol. 30, No. 5, pp. 1-8, Aug. 2020.

[22] Y. Salami, M Firouzi, "Dynamic performance of wind farms with bridge-type superconducting fault current limiter in distribution grid," 2nd International Conference on Electric Power and Energy Conversion Systems (EPECS), Sharjah, 15-17 Nov. 2011

[23] L. Chen, Ch. Deng, F. Zheng, Sh. Li, Y. Liu, Y. Liao, "Fault Ride-Through Capability Enhancement of DFIG-Based Wind Turbine With a Flux-Coupling-Type SFCL Employed at Different Locations," IEEE Transactions on Applied Superconductivity, Vol. 25, No. 3, June 2015.

[24] M. Firouzi and G. B. Gharehpetian, "Improving Fault Ride-Through Capability of Fixed-Speed Wind Turbine by Using Bridge-Type Fault Current Limiter," IEEE Transactions on Energy Conversion, Vol. 28, No. 2, pp. 361–369, June 2013.

[25] M. Firouzi, G. B. Gharehpetian, M. Pishvaei, "THD reduction of PCC voltage by using bridge-type fault current limiter," International Transaction on Electrical Energy Systems, Vol. 23, No. 5, pp. 655–668, July 2013.

[26] M. Firouzi, G. B. Gharehpetian, M. Pishvaei, "A dual functional bridge type FCL to restore PCC voltage," International Journal of Electrical Power & Energy Systems, Vol. 46, pp. 49–55. March 2013

[27] M. Firouzi, G. B. Gharehpetian, and B. Mozafari, "Improvement of Power System Stability by Using New Switching Technique in Bridge-type Fault Current Limiter," Electric Power Components and Systems, Vol. 43, pp. 234-244, 2015.

[28] H. Radmanesh, H. Fathi and G. B. Gharehpetian, "Series Transformer-Based Solid State Fault Current Limiter," in IEEE Transactions on Smart Grid, Vol. 6, No. 4, pp. 1983-1991, July 2015.

[29] M. Firouzi and G. B. Gharehpetian, "LVRT Performance Enhancement of DFIG-Based Wind Farms by Capacitive Bridge-Type Fault Current Limiter," IEEE Transactions on Energy Conversion, Vol. 9, No. 3, pp. 1118–1125, July 2018.

[30] G. Rashid, and M. H. Ali, "Transient Stability Enhancement of Double Fed Induction Machine Based Wind Generator by Bridge-Type Fault Current Limiter," IEEE Transactions on Energy Conversion , Vol. 30, No. 3, September 2015.

[31] G. Rashid, M. H. Ali, "Nonlinear Control-Based Modified BFCL for LVRT Capacity Enhancement of DFIG-Based Wind Farm," IEEE Transactions on Energy Conversion, Vol. 32, No.1, pp. 284-295, March 2017.

[32] Kh. Goweily, M. Sh. El Moursi, M. Abdel-Rahman, M. A. L. Badr, " Voltage booster scheme for enhancing the fault ride-through of wind turbines," IET Power Electronics, Vol. 8, No. 10, pp. 1853-1863, October 2015.

[33] M. Firouzi, G. B. Gharehpetian, Y. Salami, " Active and reactive power control of wind farm for enhancement transient stability of multi-machine power system using UIPC," IET Renewable Power Generation, Vol. 11, No. 8, pp. 1246-1252, July 2017.

[34] S. M. Muyeen, "A Combined Approach of Using an SDBR and a STATCOM to Enhance the Stability of a Wind Farm," IEEE Systems Journal. Vol. 9, No. 3, pp. 922–932, May 2015.

[35] M. Mahdianpoor, A. Kiyoumarsi, M. Ataei, R. Hosshmand, "Robust Implementation of Distribution Static Compensator Along With Bridge Type Fault Current Limiter for Fault Ride Through Enhancement of Fixed Speed Wind Turbines," IEEE Access, Vol. 5, pp. 14490-14501, July 2017.

[36] H. S Kartijkolaie, M Radmehr, M Firouzi, "LVRT capability enhancement of DFIG-based wind farms by using capacitive DC reactor-type fault current limiter," International Journal of Electrical Power & Energy Systems. Vol. 102, pp. 287-295, November 2018.

[37] P. M. Anderson and Anjan Bose, "Stability Simulation of Wind Turbine Systems," IEEE Transactions on Power Apparatus and Systems, Vol. PAS-102, No.12, pp. 3791-3795, December 1983

[38] S. J. Chapman, Electric Machinery and Power System Fundamentals, 5191st ed. New York, NY, USA: McGraw-Hill, pp. 310–311.

[39] M. Firouzi, S. Aslani, G. B. Gharehpetian, A. Jalilvand, "Effect of superconducting fault current limiters on successful interruption of circuit breakers," International Conference on Renewable Energies and Power Quality (ICREPQ 2012), Santiago de Compo stela, 28-30 March 2012.